'89.

GS TTL DATA BOOK

- LOW POWER SCHOTTKY TTL
- SCHOTTKY TTL

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TABLE OF CONTENTS

1. NUMERICAL/FUNCTIONAL INDEX 1-1
   A. Low Power Schottky TTLs 1-3
   B. Schottky TTLs 1-5
   C. Miscellaneous

2. FUNCTIONAL INDEX/SELECTION GUIDE 2-1

3. TTL CHARACTERISTICS
   A. Terms and Definitions 3-3
      - VOLTAGE
      - CURRENT
      - DYNAMIC CHARACTERISTICS
      - CLASSIFICATION OF CIRCUIT COMPLEXITY
      - FUNCTIONAL DESCRIPTION
      - EXPLANATION OF FUNCTION TABLES

   B. TTL Characteristics 3-7
      - TTL LOGIC FAMILY
      - INPUT CHARACTERISTICS
      - UNUSED INPUTS
      - OUTPUT CHARACTERISTICS
      - FANOUT CAPABILITY
      - NOISE MARGIN
      - OPEN COLLECT OUTPUTS

   C. Parameter Measurement Information 3-11

4. GD74LS FAMILY CIRCUITS 4-1

5. GD74S FAMILY CIRCUITS 5-1

6. QUALITY ASSURANCE MANUAL 6-1

7. ORDERING INFORMATION & PACKAGE DIMENSIONS 7-1

8. GOLDSTAR SEMICONDUCTOR SALES NETWORK 8-1

NUMERICAL/FUNCTIONAL INDEX 1
FUNCTIONAL INDEX/SELECTION GUIDE 2
TTL CHARACTERISTICS 3
GD74LS FAMILY CIRCUITS 4
GD74S FAMILY CIRCUITS 5
QUALITY ASSURANCE MANUAL 6
ORDERING INFORMATION & PACKAGE DIMENSION 7
GOLDSTAR SEMICONDUCTOR SALES NETWORK 8

A. LOW POWER SCHOTTKY TTLS

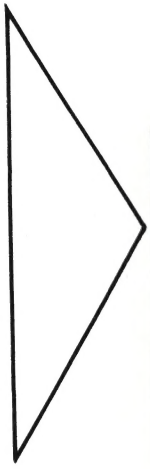
UNDER DEVELOPMENT

TYPE NO	FUNCTION	AVAILABILITY	PAGE
GD54/74LS00	Quad 2 Input NAND Gate	NOW	4-3
GD54/74LS02	Quad 2 Input NOR Gate	NOW	4-6
GD54/74LS04	Hex Invert	NOW	4-8
GD54/74LS05	Hex Invert, OC, 5.5V	NOW	4-10
GD54/74LS06	Hex Invert, OC, 30V	NOW	4-12
GD54/74LS07	Hex Buffer, OC, 30V	NOW	4-14
GD54/74LS08	Quad 2 Input AND Gate	NOW	4-16
GD54/74LS09	Quad 2 Input AND Gate, OC	NOW	4-18
GD54/74LS10	Triple 3 Input NAND Gate	NOW	4-20
GD54/74LS11	Triple 3 Inpt AND Gate	NOW	4-22
GD54/74LS14	Hex Schmitt Trigger Inverter	NOW	4-24
GD54/74LS15	Triple 3 Input AND Gate, OC	NOW	4-28
GD54/74LS16	Hex Inverter OC, 15V	NOW	4-30
GD54/74LS17	Hex Buffer, OC, 15V	NOW	4-32
GD54/74LS20	Dual 4 Input NAND Gate	NOW	4-34
GD54/74LS21	Dual 4 Input AND Gate	NOW	4-36
GD54/74LS26	Quad 2 Input NAND Gate, OC, 15V	#	4-38
GD54/74LS27	Triple 3 Input NOR Gate	NOW	4-40
GD54/74LS30	8 Input NAND Gate	NOW	4-42
GD54/74LS32	Quad 2 Input OR Gate	NOW	4-44
GD54/74LS38	Quad 2 Input AND Buffer, OC	#	4-46
GD54/74LS42	4 to 10 Decoder, BCD to Decimal	#	4-48
GD54/74LS51	AND OR Inverter Gate	NOW	4-51
GD54/74LS55	2 Wide 4 Input AND OR Invert Gate	#	4-53
GD54/74LS73	Dual JK F/F (Negative Edge)	NOW	4-55
GD54/74LS74A	Dual D Type F/F	NOW	4-58
GD54/74LS75	4 Bit Bistable Latch	NOW	4-61
GD54/74LS85	4 Bit Magnitude Comparator	#	4-63
GD54/74LS86	Quad 2 Input EOR Gate	NOW	4-67
GD54/74LS90	Decade Counter	#	4-69
GD54/74LS92	Divide by 12 Counter	#	4-72
GD54/74LS93	4 Bit Binary Counter	NOW	4-75
GD54/74LS95B	4 Bit Shift Register	#	4-78
GD54/74LS107A	Dual JK F/F	#	4-81
GD54/74LS109A	Dual JK F/F	#	4-85
GD54/74LS112	Dual JK Negative Edge F/F	NOW	4-88
GD54/74LS123	Dual Monostable Multivibrator	NOW	4-91
GD54/74LS125A	Quad Bus Buffer Gate, 3S	NOW	4-94
GD54/74LS132	Quad 2 Input NAND Schmitt Trigger	#	4-96
GD54/74LS138	3 to 8 Line Decoder/Demultiplexer	NOW	4-98
GD54/74LS139	Dual 2 to 4 Line Decoder/Demultiplexer	NOW	4-101
GD54/74LS145	BCD to Decimal Decoder/Driver	#	4-103
GD54/74LS148	8 To 3 Line Octal Priority Encoder	#	4-105
GD54/74LS151	1 of 8 Data Selector/Multiplexer	NOW	4-108
GD54/74LS153	Dual 4 to 1 Data Selector	NOW	4-111

TYPE NO	FUNCTION	AVAILABILITY	PAGE
GD54/74LS154	4 to 16 Line Decoder/Demultiplexer	NOW	4-113
GD54/74LS155	Decoder/Demultiplexer	NOW	4-111
GD54/74LS157	Quad 2 to 1 Line Data Selector	NOW	4-119
GD54/74LS158	Quad 2 to 1 Line Data Selector, Inverted	NOW	4-121
GD54/74LS161A	Sync 4 Bit Counter Binary	NOW	4-123
GD54/74LS163A	Sync 4 Bit Counter Binary, Sync Clear	NOW	4-128
GD54/74LS164	8 Bit Parllel Output Shift Reg.	NOW	4-132
GD54/74LS165	Parallel Load 8 Bit Shift Reg.	NOW	4-137
GD54/74LS166	8 Bit Shift Reg. PISO	NOW	4-141
GD54/74LS174	Hex D Type F/F	NOW	4-145
GD54/74LS175	Quad D Type F/F	NOW	4-148
GD54/74LS191	Sync Up/Down Counter, Binary	#	4-151
GD54/74LS193	Sync Up/Down Dual Clock Counter	NOW	4-156
GD54/74LS194A	4 Bit Bidirectional shift Reg.	NOW	4-162
GD54/74LS195A	4 Bit Parallel Access Shift Reg.	NOW	4-166
GD54/74LS221	Dual Monostable Multivibrator	#	4-170
GD54/74LS240	Octal Buffer, Inverted, 3S	NOW	4-176
GD54/74LS241	Octal Buffer, Noninverted, 3S	NOW	4-179
GD54/74LS242	Octal Bus Transceiver Inverted, 3S	NOW	4-182
GD54/74LS243	Quad Bus Transceiver, Noninverted, 3S	#	4-185
GD54/74LS244	Octal Buffer, Noninverted, 3S	NOW	4-188
GD54/74LS245	Octal Bus Transceiver, Noninverted 3S	NOW	4-191
GD54/74LS251	8 to 1 Line Data Select/MUX, 3S	#	4-194
GD54/74LS257A	Quad Data Selector, Noninverted, 3S	NOW	4-197
GD54/74LS258	Quad Data Selector, Inverted 3S	#	4-200
GD54/74LS259	8 Bit Addressable Latch	#	4-203
GD54/74LS273	Octal Type F/F	NOW	4-207
GD54/74LS280	9 Bit Odd/Even Parity Generator/Checker	NOW	4-210
GD54/74LS283	4 Bit Binary Full Adder	#	4-212
GD54/74LS298	Quad 2 Input MUX with Storage	#	4-216
GD54/74LS299	8 Bit Shift/Storage Register	NOW	4-218
GD54/74LS322	8 Bit Shift Reg. with Sign Extend	NOW	4-222
GD54/74LS365A	Hex Bus Driver, Noninverted 3S	NOW	4-226
GD54/74LS366A	Hex Bus Driver, Inverted, 3S	NOW	4-229
GD54/74LS367A	Hex Bus Driver, Noninverted, 3S	NOW	4-232
GD54/74LS368A	Hex Bus Driver, Inverted, 3S	NOW	4-235
GD54/74LS373	Octal D Type Latch	NOW	4-238
GD54/74LS374	Octal D Type F/F	NOW	4-241
GD54/74LS377	Octal D Type F/F	#	4-244
GD54/74LS390	Dual Decade Counter	#	4-247
GD54/74LS393	Dual 4 Bit Binary Counter	NOW	4-251
GD54/74LS395A	4 Bit Universal Shift Register, 3S	NOW	4-254
GD54/74LS541	Octal Buffer AND Line Driver, 3S	#	4-257
GD54/74LS590	8 Bit Binary Counter/Register	NOW	4-260
GD54/74LS612	Memory Mapper, 3S	NOW	4-264
GD54/74LS640	Octal Bus Transceiver, Inverted 3S	#	4-268
GD54/74LS646	Octal Bus Transceiver, Noninverted, 3S	NOW	4-272
GD54/74LS670	4 By 4 Register File, 3S	NOW	4-275
GD54/74LS688	8 Bit Magnitude Comparator	#	4-281

B. SCHOTTKY TTLS

TYPE NO	FUNCTION	AVAILABILITY	PAGE
GD54/74S00	Quad 2 Input NAND Gate	NOW	5-3
GD54/74S02	Quad 2 Input NOR Gate	NOW	5-5
GD54/74S04	Hex Inverter	NOW	5-7
GD54/74S05	Hex Inverter, OC	NOW	5-9
GD54/74S08	Quad 2 Input AND Gate	NOW	5-11
GD54/74S10	Triple 3 Input NAND Gate	NOW	5-13
GD54/74S20	Dual 4 Input NAND Gate	NOW	5-15
GD54/74S30	8 Input NAND Gate	NOW	5-17
GD54/74S32	Quad 2 Input OR Gate	NOW	5-19
GD54/74S51	AND OR Invert Gate	NOW	5-21
GD54/74S64	4-2-3-2 Input AND OR Invert Gate	#	5-23
GD54/74S74	Dual D Type F/F	NOW	5-24
GD54/74S85	4 Bit Magnitude Comparator	#	5-28
GD54/74S86	Quad 2 Input EOR Gate	NOW	5-32
GD54/74S112	Dual JK Negative Edge Triggered F/F	NOW	5-34
GD54/74S133	13 Input NAND Gate	NOW	5-37
GD54/74S138	3 to 8 Line Decoder/Demultiplexer	NOW	5-39
GD54/74S139	Dual 2 to 4 Line Decoder/Demultiplexer	NOW	5-41
GD54/74S153	Dual 4 To 1 Data Selector/multiplexer	#	5-43
GD54/74S157	Quad 2 to 1 Line Data Selector	#	5-45
GD54/74S158	Quad 2 to 1 Line Data Selector, Inverted	#	5-47
GD54/74S163A	Sync 4 Bit Counter, Binary	#	5-49
GD54/74S169A	4 Bit up/down Sync Counter, Binary	#	5-53
GD54/74S174	Hex D Type F/F	NOW	5-58
GD54/74S175	Quad D Type F/F	#	5-61
GD54/74S240	Octal Buffer, Inverted, 3S	#	5-64
GD54/74S242	Quad Bus Transceiver, Inverted, 3S	#	5-69
GD54/74S243	Quad Bus Transceiver, Noninverted, 3S	#	5-69
GD54/74S251	DATA Selector/Multiplexer, 3S	NOW	5-72
GD54/74S257	Quad Data Selector/MUX Noninverted, 3S	#	5-75
GD54/74S280	9 Bit Odd/Even Parity Generator/Checker	NOW	5-78
GD54/74S299	8 Bit Shift/Storage Register	#	5-81
GD54/74S374	Octal D Type F/F, 3S	NOW	5-85



NUMERICAL/FUNCTIONAL INDEX 1

FUNCTIONAL INDEX/SELECTION GUIDE 2

TTL CHARACTERISTICS 3

GD74LS FAMILY CIRCUITS 4

GD74S FAMILY CIRCUITS 5

QUALITY ASSURANCE MANUAL 6

ORDERING INFORMATION & PACKAGE DIMENSION 7

GOLDSTAR SEMICONDUCTOR SALES NETWORK 8

FUNCTIONAL INDEX/SELECTION GUIDE

Function	Type of output		Type No	Typical propagation delay time (ns)	Typical power Dissipation per gate(mw)	package	Page
	Totem pole	open-collector					
1. INVERTERS and NAND GATES							
Quad 2 Input NAND	o		54/74LS00	8,5	2	14 DIP	4-3
	o		54/74S00	3	19	14 DIP	5-3
	o		54/74LS26	16	2	14 DIP	4-38
Triple 3 Input NAND	o		54/74LS10	9.5	2	14 DIP	4-20
	o		54/74S10	3	19	14 DIP	5-13
Dual 4 Input NAND	o		54/74LS20	9.5	2	14 DIP	4-34
	o		54/74S20	3	19	14 DIP	5-15
8 Input NAND	o		54/74LS30	10.5	2.4	14 DIP	4-42
	o		54/74S30	6	21.25	14 DIP	5-17
13 Input NAND	o		54/74S133	6	21.25	16 DIP	5-37
Hex Inverter	o		54/74LS04	9.5	2	14 DIP	4-8
	o		54/74S04	3	19	14 DIP	5-7
Hex Inverter		o	54/74LS05	16	2	14 DIP	4-10
		o	54/74S05	5	17.5	14 DIP	5-9
2. NOR GATES							
Quad 2 Input	o		54/74LS02	10	2.75	14 DIP	4-6
	o		54/74S02	3.5	29	14 DIP	5-5
Triple 3 Input	o		54/74LS27	10	4.5	14 DIP	4-40
3. AND GATES							
Quad 2 Input	o		54/74LS08	12	4.25	14 DIP	4-16
	o		54/74S08	4.75	32	14 DIP	5-11
		o	54/74LS09	20	4.25	14 DIP	4-18
Triple 3 Input	o		54/74LS11	12	4.25	14 DIP	4-22
		o	54/74LS15	20	4.25	14 DIP	4-28
Dual 4 Input		o	54/74LS21	12	4.25	14 DIP	4-36
4. OR GTES							
Quad 2 Input	o		54/74LS32	12	5	14 DIP	4-44
	o		54/74S32	4	35	14 DIP	5-19
5. EXCLUSIVE OR GATES							
Quad 2 Input	o		54/74LS86	10	30	14 DIP	4-67
	o		54/74S86	7	250	14 DIP	5-32

6. AND-OR-INVERT GATES

Dual 2-Wide 2/3 Input	o		54/74LS51	12.5	2.75	14 DIP	4-51
	o		54/74 S51	3.5	28	14 DIP	5-21
2 Wide 4 Input	o		54/74LS55	12.3	2.75	14 DIP	4-53
4 Wide 4-2-3-2 Input	o		54/74 S64	3.5	29	14 DIP	5-23

7. BUFFERS/LINE DRIVERS

I: With Inverted Output, N: With Noninverted Output

Function	Type of Output			Type No.	Typ Propaga -tion Delay Time (ns)	Max Source Current (mA)	Max Sink Current (mA)	Package	Page
	totem pole	open collector	3-State						
Octal Buffers/Line Drivers			I	74LS240	10	−15	24	20 DIP	4-176
			I	54LS240	10	−12	12	20 DIP	4-176
			I	74S240	5	−15	64	20 DIP	5-64
			I	54S240	10	−12	48	20 DIP	5-64
			N	74LS241	10	−15	24	20 DIP	4-179
			N	54LS241	10	−12	12	20 DIP	4-179
			N	74LS244	10	−15	24	20 DIP	4-188
			N	54LS244	10	−12	12	20 DIP	4-188
			N	74LS541	9.5	−15	24	20 DIP	4-257
			N	54LS541	9.5	−12	12	20 DIP	4-257
Hex Buffers/Line Drivers			N	74LS365	9.5	−2.6	24	16 DIP	4-226
			N	54LS365	9.5	−1	12	16 DIP	4-226
			I	74LS366	9.5	−2.6	24	16 DIP	4-229
			I	54LS366	9.5	−1	12	16 DIP	4-229
			N	74LS367	9.5	−2.6	24	16 DIP	4-232
			N	54LS367	9.5	−1	12	16 DIP	4-232
			I	74LS368	9.5	−2.6	24	16 DIP	4-235
			I	54LS368	9.5	−1	12	16 DIP	4-235
Quad Bus Buffers/Drivers			N	74LS125	8	−2.6	24	14 DIP	4-94
			N	54LS125	8	−1	12	14 DIP	4-94
Quad Transceiver			I	74LS242	11	−15	24	14 DIP	4-182
			I	54LS242	11	−12	12	14 DIP	4-182
			I	74S242	5.5	−15	64	14 DIP	5-69
			I	54S242	5.5	−12	48	14 DIP	5-69
			N	74LS243	12	−15	24	14 DIP	4-185
			N	54LS243	12	−12	12	14 DIP	4-185
			N	74S243	5.5	−15	64	14 DIP	5-69
			N	54S243	6.0	−12	48	14 DIP	5-69
Quad 2-Input NAND Buffer		I		74LS38	19	24		14 DIP	4-46
		I		54LS38	19	—		14 DIP	4-46

Function	Type of Output			Type No	Typ Propaga -tion Delay Time (ns)	Max Source Current (mA)	Max Sink Current (mA)	Package	Page
	totem pole	open collector	3-State						
Octal Transceiver			N	74LS245	12	−16	24	20 DIP	4-191
			N	54LS245	12	−12	12	20 DIP	4-191
			I	74LS640	7	−15	24	20 DIP	4-268
			I	54LS640	7	−12	48	20 DIP	4-268
			N	74LS646	12.5	−15	24	24 DIP	4-272
			N	54LS646	12.5	−12	12	20 DIP	4-272

I: With Inverted Output, N: With Noninverted Output

8. SCHMITT TRIGGER NAND GATES/INVERTS

Function	Type of output		Type No	Typical Delay Time(ns)	Typical Hysteresis	Package	Page
	totem pole	3-state					
Hex S/T Inverts	0		54/74LS14	15	0.8	14 DIP	4-24
Quad 2-Input NAND S/T	0		54/74LS132	15	0.8	14 DIP	4-96

9. J-K FLIP/FLOPS

Function	Type No	Clock Edge	Data Times		Typical Characteristics		Package	Page
			Setup (ns)	Hold (ns)	f_{max} (MHz)	PW/FF (mW)		
Dual J/K with Clear	54/74LS73	↓	20	0	45	20	14 DIP	4-55
	54/74LS107	↓	20	0	45	10	14 DIP	4-81
Dual J/K with Set & Clear	54/74LS112	↓	20	0	45	10	16 DIP	4-88
	54/74S112	↓	3	0	125	75	16 DIP	5-34
Dual J/$\overline{K}$ with Set & Clear	54/74LS109	↑	20	5	33	10	16 DIP	4-85

↓ Negative Edge ↑ Positive Edge

10. D TYPE FLIP/FLOPS

Function	Type No	Clock Edge	Data Times		Typical Characteristics		Package	Page
			Setup (ns)	Hold (ns)	f_{max} (MHz)	PW/FF (mW)		
Dual with Set a Clear	54/74LS74	↑	25	5	33	10	14 DIP	4-58
	S74	↑	3	2	110	75	14 DIP	5-24
Hex D Type with Clear	54/74LS174	↑	20	5	40	10.6	16 DIP	4-145
	S174	↑	5	3	110	75	16 DIP	5-58
Duad Q and Q outputs	54/74LS175	↑	20	5	40	10.6	16 DIP	4-148
	S175	↑	5	3	110	75	16 DIP	5-61
Octal D Type with Clear	54/74LS273	↑	20	5	40	10.6	20 DIP	4-207

Function	Type No	Clock Edge	Data Times		Typical Characteristics		Package	Page
			Setup (ns)	Hold (ns)	f_{max} (MHZ)	PW/FF (mW)		
Octal D Type, 3S	54/74LS374	↑	20	0	50	17	20 DIP	4-241
	54/74 S374	↑	5	2	100	56	20 DIP	
Octal D Type, with Enable	54/74LS377	↑	20	5	40	10.6	20 DIP	4-244

11. LATCHES, REGISTERS

Function	Type No.	En-able	Pre-Set	Typ Delay Time(ns)	Typ Power Diss(mW)	No.of Bits	Outputs	Package	Page
Dual 2-Bit with Indep Enable	54/74LS75	⎍	—	11	32	4	Q,Q	16 DIP	4-61
Transparent	54/74LS373	⎍	—	19	120	8	Q	20 DIP	4-238
Addressable	54/74LS259	—	⎎	17	110	8	Q	16 DIP	4-203

⎍ : Active high Level ⎎ : Active Low Level

12. SHIFT REGISTERS

Function	Type No	No of Bits	Shift Freq (MHz)	Modes				Package	Page
				S-R	S-L	Load	Hold		
Parallel In Parallel Out (Bidirectional)	54/74LS299	8	25	o	o	o	o	20 DIP	4-218
	54/74S299	8	50	o	o	o	o	20 DIP	5-86
	54/74LS194A	4	25	o	o	o	o	16 DIP	4-162
Parallel In Parallel Out	54/74LS322	8	30	o	—	o	o	20 DIP	4-222
	54/74LS195	4	30	o	—	o	—	16 DIP	4-166
	54/74LS395A	4	30	o	—	o	—	16 DIP	4-254
	54/74LS95	4	30	o	—	o	—	14 DIP	4-78
Serial In/Parallel Out	54/74LS164	8	25	o	—	—	—	14 DIP	4-132
Parallel-In/Serial Out	54/74LS165	8	25	o	—	—	—	16 DIP	4-137
	54/74LS166	8	25	o	—	—	—	16 DIP	4-141

13. ASYNCHRONOUS COUNTERS

Function	Type No	Count freq (MHz)	Parallel Load	Trigger	Clear	Package	Page
Decade	54/74LS90	32	Set to 9	↓	⎍	14 DIP	4-69
4 Bit	54/74LS93	32	None	↓	⎍	14 DIP	4-75
Divide By 12	54/74LS92	32	None	↓	⎍	14 DIP	4-72
Dual Decade	54/74LS390	25	None	↓	⎍	16 DIP	4-247
Dual 4 Bit Binary	54/74LS393	25	None	↓	⎍	14 DIP	4-251

14. SYNCHRONOUS COUNTERS

Function	Type No	Count freq (MHz)	Parallel Load	Trigger	Clear	Package	Page
4 Bit Binary	54/74LS161A	25	Sync	↑	Async-L	16 DIP	4-123
	54/74LS163A	25	Sync	↑	Sync-L	16 DIP	4-128
	54/74S163A	40	Sync	↑	Sync-L	16 DIP	5-49
4 Bit Binary UP/Down	54/74LS191	20	Async	↑	None	16 DIP	4-151
	54/74LS193	25	Async	↑	Aync-H	16 DIP	4-156
	54/74S169	40	Sync	↑	Sync-L	16 DIP	5-53

15. MONOSTABLE MULTIVIBRATORS

Function	Type No	Direct Clear	Output Pulse Range	Typ Total Power	Package	Page
Dual	54/74LS123	Yes	116ns-∞	60mW	16 DIP	4-91
	74LS221	Yes	20ns-70s	119mW	16 DIP	4-170
	54LS221	Yes	20ns-49s	119mW	16 DIP	4-170

16. COMPARATOR

Function	Type No	Typical Compare time(ns)	Typ Total Power Dissipation(mW)	Package	Page
4 Bit Magnitude	54/74LS85	11.5	365	16 DIP	4-63
	54/74S85	25	52	16 DIP	5-28

17. DATA SELECTORS/MULTIPLEXERS

Function	Type No	Type of Output	Typical Delay Times			Package	Page
			Data to INV Output	Data to NONINV Output	From Enable		
8 Line To 1 Line	54/74LS151	2S	11	18	27	16 DIP	4-108
	54/74LS251	3S	17	21	21	16 DIP	4-194
	54/74S251	3S	4.5	8	14	16 DIP	5-72
Dual 4 Line To 1 Line	54/74LS153	2S	—	14	17	16 DIP	4-111
	54/74S153	2S	—	6	9.5	16 DIP	5-43
Quad 2 Line To 1 Line	54/74LS157	2S	—	9	14	16 DIP	4-119
	S157	2S	—	5	8	16 DIP	5-45
	54/74LS158	2S	7	—	12	16 DIP	4-121
	S158	2S	4	—	7	16 DIP	5-47
	54/74LS257	3S	—	12	20	16 DIP	4-197
	S257	3S	—	5	14	16 DIP	5-75
	54/74LS258	3S	12	—	20	16 DIP	4-200
Quad 2 To 1, with Storage	54/74LS298	2S	—	20	—	16 DIP	4-216

18. DECODERS/DEMULTIPLEXERS

Function	Type No	Type of Output	Typ Select Time (ns)	Typ Enable Time (ns)	Package	Page
4 Line To 16 Line	54/74LS154	Totempole	23	19	24 DIP	4-113
4 Line To 10 Line	54/74LS42	"	17	—	16 DIP	4-48
3 Line To 8 Line	54/74LS138	"	22	21	16 DIP	4-98
	54/74 S138	"	8	7	16 DIP	5-39
Dual 2-Line To 4 Line	54/74LS139	"	22	19	16 DIP	4-101
	54/74 S139	"	7.5	6	16 DIP	5-41
	54/74LS155	"	18	15	16 DIP	4-116

19. PRIORITY ENCODERS

Function	Type No	Typ delay Time	Typ Power Diss	Package	Page
Cascadable Octal	54/74LS148	15ns	60mW	16 DIP	4-105

20. ADDER

Function	Type No	Typ delay Time		Typ Power Diss	Package	Page
		Carry Time	Add Time			
Single 4-Bit Full ADDER	54/74LS283	11ns	15ns	24mW	16 DIP	4-212

21. PARITY GENERATOR/CHECKER

Function	Type No	Typ delay Time	Typ Power Diss	Package	Page
9 Bit Odd/Even Parity Gen/ Checker	54/74LS280	31ns	80mW	14 DIP	4-210
	54/74S280	13ns	335mW	14 DIP	5-78

22. REGISTER FILES

Function	Type No	Typ power Diss	Typ delay Time		Package	Page
			Write Time	Read Time		
4 By 4, with 3S Output	54/74LS670	135mw	24ns	19ns	20 DIP	4-275

NUMERICAL/FUNCTIONAL INDEX 1

FUNCTIONAL INDEX/SELECTION GUIDE 2

TTL CHARACTERISTICS 3

GD74LS FAMILY CIRCUITS 4

GD74S FAMILY CIRCUITS 5

QUALITY ASSURANCE MANUAL 6

ORDERING INFORMATION & PACKAGE DIMENSION 7

GOLDSTAR SEMICONDUCTOR SALES NETWORK 8

A. TERMS AND DEFINITIONS

VOLTAGES

V_{IH} High-level input voltage
An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Low-level input voltage
An input voltage level with the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{T+} Positive-going threshold voltage
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltagbe, V_{T-}.

V_{T-} Negative-going threshold voltage
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

V_{OH} High-level output voltage
The voltage at an output terminal for a specified output current I_{OH} with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} Low-level output voltage
The voltage at an output terminal for a specified output current I_{OL} with input conditions applied that according to the product specification will establish a low level at the output.

$V_{O(on)}$ On-state output voltage
The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the on state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

$V_{O(off)}$ Off-state output voltage
The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This characteristics is ususally specified only for outputs not having internal pull-up elements.

CURRENT

I_{IH} High-level input current
The current flowing into* an input when a specified high-level voltage is applied to that input.

I_{IL} Low-level input current
The current flowing into* an input when a specified low-level voltage is applied to that input.

I_{OH} High-level output current
The current flowing* the output with a specified high-level output voltage V_{OH} applied.

Note: This parameter is usually specified for open-collector outputs intended to drive other logic circuits.

* Current flowing out of a terminal is a negative value.

I_{OL} Low-level output current
The current flowing the output with a specified Low-level output voltage V_{OL} applied.

$I_{O(off)}$ Off-state output current
The current flowing into* an output with a specified output voltage applied and input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits or for three-state outputs.

I_{OS} Short-circuit output current
The current flowing into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified) potential).

I_{CCH} **Supply current, output(s) high**
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a high-level voltage.

I_{CCL} **Supply current, output(s) low**
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a low-level voltage.

DYNAMIC CHARACTERISTICS

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause a change of output state with each clock pulse.

t_{PHZ} **Output disable time (of a three-state output) from high level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLZ} **Output disble time (of a three-state output) from low level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PHL} **Propagation delay time, high-to-low-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{TLH} **Transition time, low-to-high-level output**
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

t_{THL} **Transition time, high-to-low-level output**
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

t_w **Average pulse width**
The time between 50-percent-amplitude points on the leading and trailing edges of a pulse.

t_{hold} **Hold time**
The time interval for which a signal or pulse is retained at a specified input terminal after an active transition occurs at another specified input terminal.

* Current flowing out of a terminal is a negative volue.

$t_{release}$ **Release time**
The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.

t_{setup} **Setup time**
The time interval for which a signal is applied and maintained at a specified input terminal before an active transition occurs at another specified input terminal.

t_{PZH} **Output enable time (of a three-state output) to high level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing form a high-impedance (off) state to the defined high level.

t_{PZL} **Output enable time (of a three-state output) to low level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output chaning from a high-impedance (off) state to the defined low level.

CLASSIFICATION OF CIRCUIT COMLEXITY

Gate equivalent circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

LSI **Large-scale integration**

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether logical or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

MSI **Medium-scale integration**

A concept whererby a complete subsystem or system fucntion is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

SSI **Small-scale integration**

Integrated circuits of less complexity than medium-scale integration (MSI)

FUNCTIONAL DESCRIPTIONS

Buffer: A logic gate with high output drive capability, or fan-out. Buffers are used where a. single circuit must drive a large number of loads.

Comparator: A logic circuit that will compare two separate input signals and produce an output based on that comparison. A simple comparator is the Exculsive-NOR gate, which produces a high level output only when its two inputs are identical.

Counter: A logic circuit that counts the number of input pulses it receives. Counters can be used for frequency division, counting, and sequencing digital operations. Common counter configurations are Binary, where the device counts from 0 to 15 and Decade, where the device counts from 0 to 9.

Data Selector/Multiplexer: A logic circuit that will select one of several input signals and feed that signal onto a common bus line. It can be thought of as a multipole, multiposition switch with each switch pole representing one output and each switch position representing one input.

Decoder/Demultiplexer: A logic circuit that is the complement of the Data Selector/Multiplexer; that is, this circuit takes an input signal and feeds it to any one of several output lines depending on the information placed on its steering, or control, inputs.

Driver: Same as Buffer, above.

Flip-Flop: A logic circuit that is used to store information. A flip-flop is called "bistable" since it has two stable states.

Gate: The basic building block of all logic circuits; an element whose output is a Boolean function of its inputs. The basic functions are the AND, OR, and NOT. By combining these functions, NAND, NOR, and Exclusive-OR and Exclusive-NOR gates are built.

Latch: A bistable element that latches, or holds, data which is present at its input at the time the Enable input goes to its inactive state. When the Enable input is active, the data, present at the input, is passed directly to the output, similar to the operation of a gate.

One-Shot: Monostable multivibrator; a flip-flop that only has one stable state. When triggered by an input transient, it flips to its unstable state for a time period determined by an external R-C network connected to its timing inputs, and then returns to its stable state.

Shift Register: A series of flip-flops in which the data signal is shifted out of one flip-flop and into the succeeding flip-flop during an active transition on the clock input.

Transceiver: A logic circuit that can transmit data onto a bus line and receive data off of the bus line using the same terminal as an input and output. The direction of signal flow is determined by logic levels present at a Direction Control input.

Other Terms

Asynchronous: A mode of operation that does not require any specific timing relationship between different control inputs.

Open Collector: Output configuration that has no internal pullup. This configuration enables outputs that are connected together (wire-OR) to assume opposite states without incurring damage.

Schmitt Trigger: An input configuration that has a different threshold point depending on whether the input signal is rising or falling. This is especially useful in electrically noisy environments.

Synchronous: A mode of operation where specific timing requirements must be met between control inputs before an indicated action can occur.

Totem Pole: An output configuration that contains an internal pullup structure, usually a transistor pullup allowing higher output drive capability than is available with open collector outputs.

TRI-STATE: A registered trademark for a circuit configuration in which the device output can be switched 'off' during which time the output presents a very high impedance to the bus it is connected to. this allows multiple outputs to be connected to a bus line while only one output drives the line, the other outputs being switched into their high impedance states.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in the function tables found in data sheets:

H	=	high logic level(steady state)
L	=	low logic level (steady state)
↑	=	transition from low to high logic level
↓	=	transition from high to low logic level
X	=	irrelevant (any level, including transitions)
Z	=	off (high impedance) state of a TRI-STATE output
a...h	=	the level of steady state inputs at inputs A through H respectively
Q_o	=	the level of Q before the indicated steady state input conditions were established
$\overline{Q}_o$	=	complement of Q_o or level of Q before the indicated steady state input conditions were established
Q_n	=	level of Q before the most recent active transtion indicated by ↑ or ↓
⎍	=	one high level pulse
⎎	=	one low level pulse
toggle	=	each output changes to te complement of its previous level on each active transition indicated by ↑ or ↓

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

B. TTL CHARACTERISTICS

1. TTL LOGIC FAMILY

Series 54/74 transistor-transistor logic has, since its introduction in 1965, become the most popular digital intergrated cirucit logic family ever offered and is probably the easiest to use medium-to-high performance logic circuits available.

Digital integrated circuits have historically been characterised for both speed and power, Each families have advantages and disadvantages over the previos families. Today Gold Star Semiconductor provides two basic bipolar logic families.

Low Power Schottky (GD 54/74 LSxxx)
Schottky (GD 54/74 Sxxx)

1) Low Power Schottky

Low-power Schottky TTL integrated circuits are now firmly established as the standard logic configuration for new high performance system designs. They have essentially entirely replaced standard "gold-doped" TTL devices in all applications. In addition, they have relegated the other logic speed (ECL) or low power for battery operated operation (CMOS) is mandatory.

GD 54/74LS Series
- Typical tpd 9.5ns/gate at 2mw
- Typical Register fmax = 40 MHz

The first application of the low power technology to a commercially available product was to redesign the most popular elements of the standard, gold-doped 54/74 TTL family in LS. This provided a set of functions pin-for-pin and speed compatible with the earlier TTL parts, but requiring as little as 20% of the power. The basic gate design for a 54LS/74LS element is shown in Figure 1. This offers a typical propagation delay of 10ns at 2mW power dissipation. Similar improvements have been made in power requirements for flip-flops and MSI functions.
This LS family offers many advantages to the system designers over the older standard TTL functions.

- Lower supply currents permit the use of smaller, lower cost power supplies.
- Reduced power dissipation generates less heat and simplifies cooling needs and allows increased board packing density.
- Lower on-chip operating temperatures decrease IC failure rates, thus improving system reliability.
- Lower operating currents reduce outputs spiking, leading to a decrease in noise generation and associated system problems.
- As the input load current requirements of Low-Power Schottky are only 25% of standard TTL, the new circuits are easier to interface with MOS elements, such as memories and microprocessors.

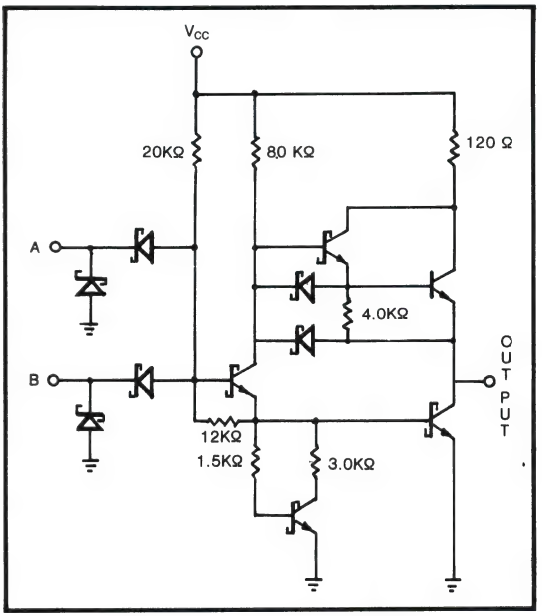


Figure 1. GD 74LS TTL Gate

- Provided input and output loading rules are obeyed, as the functions and pin-outs are identical to those of the earlier TTL families, it is easy to upgrade existing systems.

2) Schottky

This family features the high switching speed of unsaturated bipolar emitter-coupled logic, but consumes more power than standard TTL devices.

GD54/74 S Series
- Typical tpd 3ns/gate at 20 mw
- Typical Register fmax = 70 MHz

To achieve this high speed, the schottky barrier diode is incorporated as a clamp to divert the excess base current and to prevent the transistor from reaching deep saturation.

2. INPUT CHARACTERISTICS

Figure 3-1 shows the input characteristics of an LS-TTL circuit. Input diode breakdown is typically greater than 15V and input leakage current above 1.5V is negligible. As the input voltage falls below 1.3V, gate current starts flowing out of the input, denoting the transition region. For input voltage between 1.0V and −0.3V, the I-V charcteristics has the slope of the 24KΩ gate pull-up resistor. The clamping diode conducts and the current increases rapidly when the input voltage goes below about −0.3V. Typical transfer characteristics can be found in Figure 3-2 and input threshold variation with tamperature information is provied in Table 3-1.

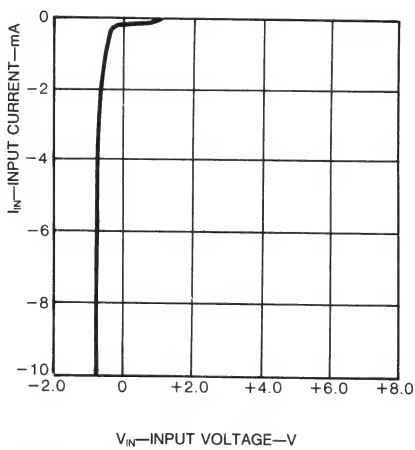


Fig. 3-1 LS-TTL Input Characteristics Figure

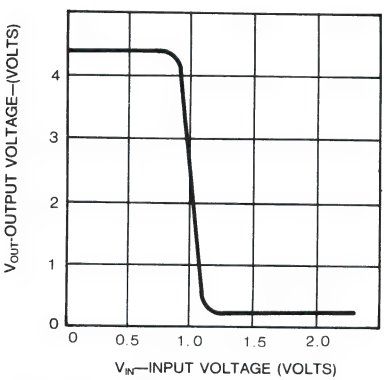


Fig. 3-2 Typical Output vs Input Voltage Characteristic

TYPE	−55°C	+25°C	+125°C
S	1.5	1.3	1.1
LS	1.2	1.0	0.8

TABLE 3-1

TYPICAL INPUT THRESHOLD VARIATION WITH TEMPERATURE

3. UNUSED INPUTS

An unused input to an AND or NAND gate should not be left floating as it can act as an antenna for noise. On devices with storage, such as latches, registers and counters, it is particularly important to terminate unused inputs (MR, PE, PL, CP) properly since a noise spike on these inputs might change the contents of the memory. This technique optimizes switching speed as the distributed capacitance associated with the floating input, bond wire and package leads is eliminated. To terminate, the input should be held between 2.4V and the maximum input voltage. One method of achieving this is to connect the unused input to V_{CC}. Most LS inputs have a breakdown voltage >7V and require no series resistor. Devices specified with a maximum 5.5 volt breakdown should use a 1kΩ to 10kΩ current limiting series resistor to protect against V_{CC} transients. Another mehtod is to connect the unused input to the output of an unused gate that is forced HIGH. Do not connect an unused input to another input of the same NAND or AND function. Although recommended for standard TTL with LS this increases the input coupling capacitance and reduces A.C. noise immunity.

4. OUTPUT CHARACTERISTICS

The typical V_{OL} versus I_{OL} characteristics of LS devices are shown in Figure 5-1. MOST 74LS functions are specified at V_{OL}=0.4V at I_{OL}=4mA and 0.5V at 8mA. Some newer designs are being guaranteed at I_{OL} of 12mA and 24mA. The typical V_{OH} versus I_{OH} curves are shown in Figure 5-2.

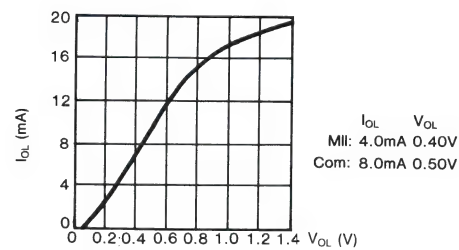


Figure 5-1 V_{OL} vs I_{OL} Typical LS Device Curve

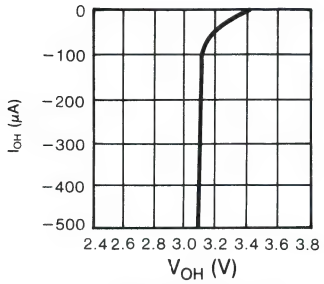


Figure 5-2 V_{OH} vs I_{OH} Typical Is Device Curve

5. FAN OUT CAPABILITY

The fan-out capability of a logic family indicates the number of inputs which can be driven by a single output. The input and output loding parameter of all families are defined as follow.

1 TTL Unit Load(U.L) = 40μA in the High State (Logic H)

1 TTL Unit Load(U.L) = 1.6mA in the Low State (Logic L)

PINS	54/74 S(U.L) HIGH / LOW	54/74 LS(U.L) HIGH / LOW
Inputs Outputs	1.25 / 1.25 25 / 12.5	0.5 / 0.25 10 / 5.0

Example) Input Load.

* The GD74LS00 gate which has an I_{IL} of 0.4mA and an I_{IH} of 20μA, has an input Low load factor of

$$\frac{0.4\ mA}{1.6\ mA} = 0.25\ U.L.$$

an input High Load factor of

$$\frac{20\ \mu A}{40\ \mu A} = 0.5\ U.L.$$

Example) Output Load

* The output of the GD74LS00 gate will sink 8.0 mA in the Low State and SOUIRCE 400 μA in the High State. The normalized output Low driver factor is

$$\frac{8.0\ mA}{1.6\ mA} = 5.0\ U.L$$

and the output High driver factor is

$$\frac{400\ \mu A}{40\ \mu A} = 10\ U.L.$$

6. NOISE MARGIN

The D.C. Noise margin of a digital system are defined as follows.

Logic High Noise Margin = V_{OH} - V_{IH}
Logic Low Noise Margin = V_{IL} - V_{OL}

These parameters for LS devices are shown Table 6-1

PARAMETERS	54LS/74LS LOW-POWER SCHOTTKY					
	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	I_{OL}=4.0mA				0.4	V
	I_{OL}=8.0mA (COM'L only)				0.5	
V_{OH}	I_{OH}=−400μA	MIL	2.5	3.4		V
		COM'L	2.7	3.4		
V_{IL}	Logic Low	MIL			0.7	V
		COM'L			0.8	
V_{IH}	Logic High		2.0			V
I_{IL}	V_{IN}=0.4V				−0.38	mA
I_{IH}	V_{IN}=2.7V				20	μA

Table 6-1a

PARAMETER	54S/74S SCHOTTKY TTL					
	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	I_{OL}=20mA			0.3	0.5	V
V_{OH}	I_{OH}=−1.0mA	MIL	2.5	3.4		V
		COM'L	2.7	3.4		
V_{IL}	Logic LOW				0.8	V
V_{IH}	Logic HIGH		2.0			V
V_{IL}	V_{IN}=0.5V				−2.0	mA
I_{IH}	V_{IN}=2.7V				50	μA

Table 6-2a

Table 6-2 compares the guaranteed noise margin values for the LS and S devices.

Table 6-2a
LOW Level Noise Margins (Military)

From \ To	LS	S	Units
LS	300	400	mV
S	200	300	mV

From V_{OL} to V_{IL}

Table 6-2b
HIGH Level Noise Margins (Military)

From \ To	LS	S	Units
LS	500	500	mV
S	500	500	mV

From V_{OH} to V_{IH}

Table 6-2c
LOW Level Noise Margins (Commercial)

From \ To	LS	S	Units
LS	700	700	mV
S	700	700	mV

From V_{OH} to V_{IH}

Table 6-2d
HIGH Level Noise Margins (Commercial)

From \ To	LS	S	Units
LS	300	300	mV
S	300	300	mV

From V_{OL} to V_{IL}

7. Open Collector Outputs

Open-collector devices are totem pole outputs where the upper output (usually a Darlington transistor) is left out of the circuit. As such, these devices have no active logic high drive and cannot be used to drive a line high. The advantage to open-collector devices is that a number of outputs can be directly tied together.

When dealing with open-collector devices, it must be noted that each output requires a resistive pull-up, usually tied to V_{CC}. (By using high voltage outputs, one can tie the resistor pull-up to a voltage higher than V_{CC}.) Desingers often try to get away with tying the output to an input and relying on the I_{IL} curent to pull up the output. This is unwise, as it is just like leaving inputs floating: the input is very susceptible to noise and can easily give false signals. Shown below are two equations that can be used to determine the min/max range of the pull-up resistor.

$$R_{MAX}=\frac{(V_{CC(MIN)}-V_{OH})}{(N1\cdot I_{OH}+N2\cdot I_{IH})}$$

$$R_{MIN}=\frac{(V_{CC(MIN)}-V_{OL})}{(I_{OL}-N2\cdot I_{IL})}$$

whree: N1 = the number of open-collector devices tied together,
N2 = the number of inputs being driven on the line.

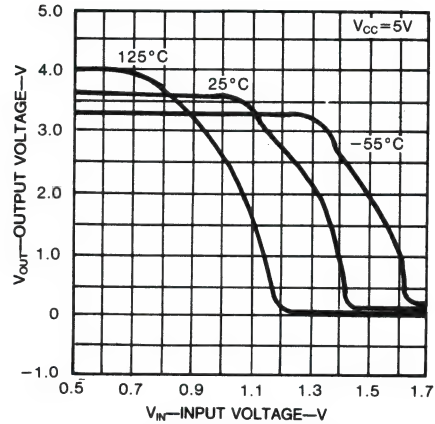


FIG. 6-1 VOLTAGE TRANSFER FUNCTION OF AN S-TTL GATE

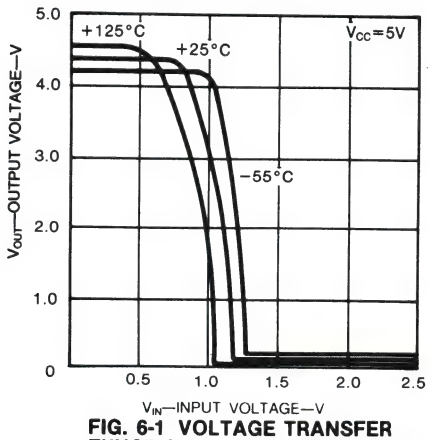
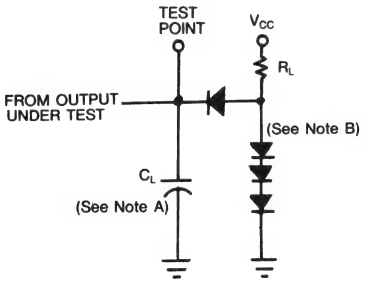


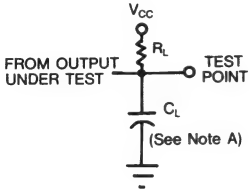
FIG. 6-1 VOLTAGE TRANSFER FUNCTION OF AN LS-TTL GATE

Figure 6-1 and 6-2 shows the transfer characteristics of S-TTL, LS-TTL inverting gates, respectively. The steepest part of a particular curve, where the output changes rapidly, for small changes in input, is called the threshold voltage input signals above or below this region cause little or no change in output and thus are of no concern. Problems can occur when an input voltage, where steady-state, transient or a combination of both, causes an output voltage to rise or fall into the threshold region of its driven loads. Thus, noise of check this magnitude can propagate, which is a useful criterion.

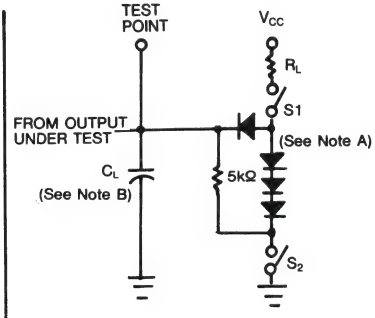
C-1. PARAMETER MEASUREMENT INFORMATION (GD74LS DEVICES)



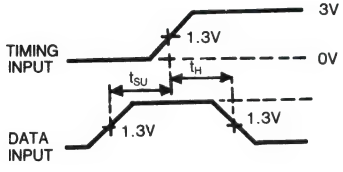
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



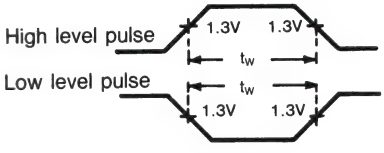
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



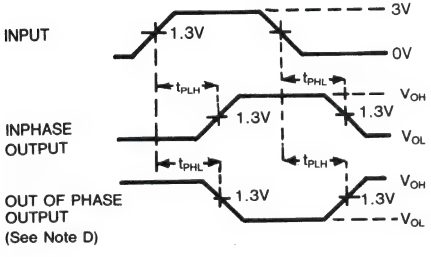
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



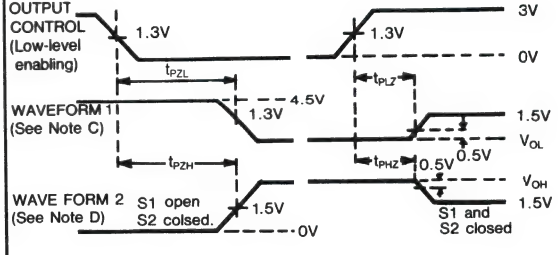
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



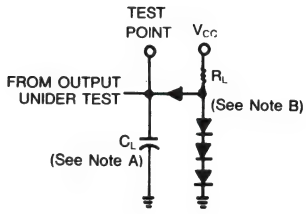
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE STATE OUTPUTS

NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that output is high encept when disabled by the output control.

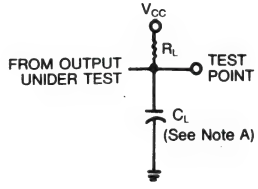
NOTES: D. When measuring propagation dealy times of 3-state outputs, switches S_1 and S_2 are closed.

NOTES: E. All input pulses are supplied by generators having the following characteristics: PRR≤1 MHz, Z_{out}≈50Ω and: For Series 54LS/74LS, t_r≤15 ns, t_f≤6 ns.

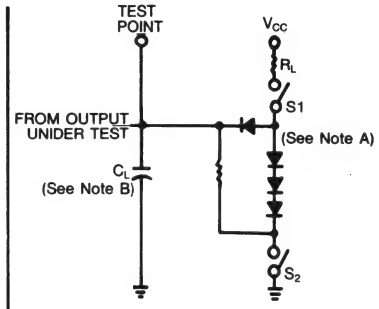
C-1. PARAMETER MEASUREMENT INFORMATION (GD74S DEVICES)



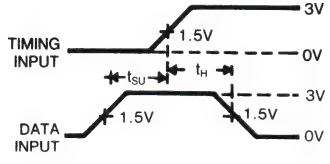
LOAD CIRCUIT FOR
BISTATE
TOTEM-POLE OUTUTS



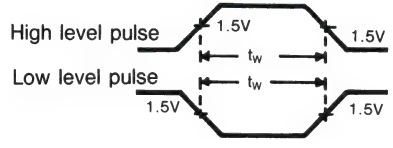
LOAD CIRCUIT FOR
OPEN-COLLECTOR OUTPUTS



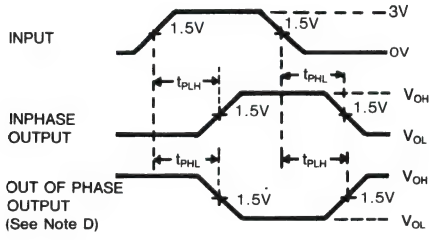
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



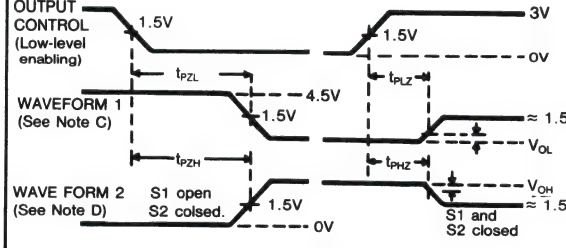
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES:

A. C_L includes probe and lig capacitance
B. All diodes are 1N916 or 1N3064.
C. Waveform 1 is for an output with internal conditions such that the output is low except whern disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.
F. All input pulses are supplied by generators having the following characteristics: PRR≤1 MHz, Z_{out}≈50Ω and: For Series 54S/74S, t_r≤2.5 ns, t_f≤2.5 ns.

NUMERICAL/FUNCTIONAL INDEX 1

FUNCTIONAL INDEX/SELECTION GUIDE 2

TTL CHARACTERISTICS 3

GD74LS FAMILY CIRCUITS 4

GD74S FAMILY CIRCUITS 5

QUALITY ASSURANCE MANUAL 6

ORDERING INFORMATION & PACKAGE DIMENSION 7

GOLDSTAR SEMICONDUCTOR SALES NETWORK 8

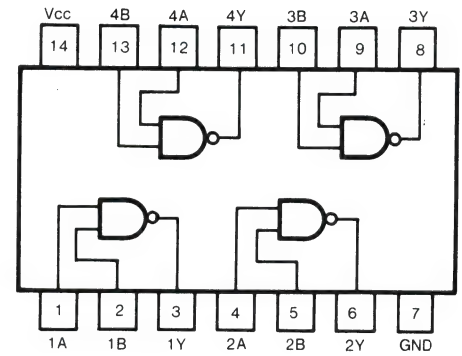
GD54/74LS00

QUADRUPLE 2-INPUT POSITIVE NAND GATES

Description

This device contains four independent 2-input NAND gates. It performs the Boolean functions $Y=\overline{A \cdot B}$ or $Y=\overline{A}+\overline{B}$ in positive logic.

Pin Configuration

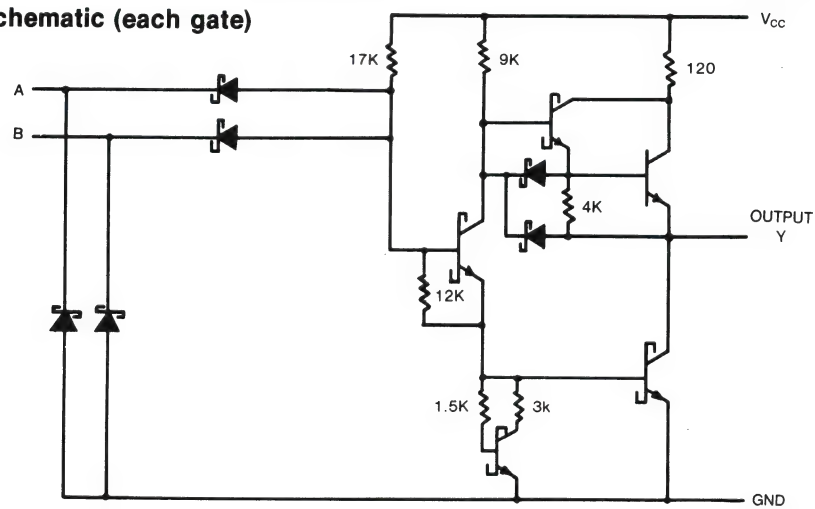


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

Circuit Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max,	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	μA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max			0.8	1.6	mA
I_{CCL}		Total with outputs low	V_{CC}=Max			2.4	4.4	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed ond second.

Switching Characteristics, V_{CC}=5V, T_A=25°C

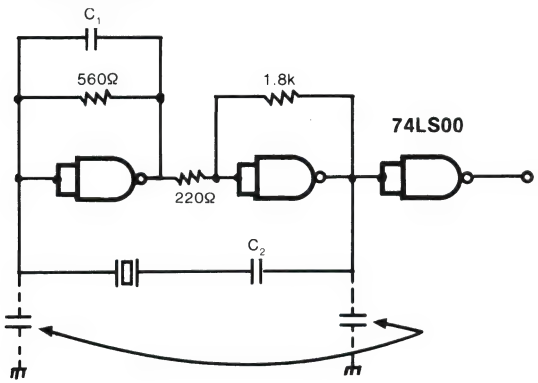
SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	15	ns

#For load circuit and voltage waveforms, see page 3-11.

Application Example

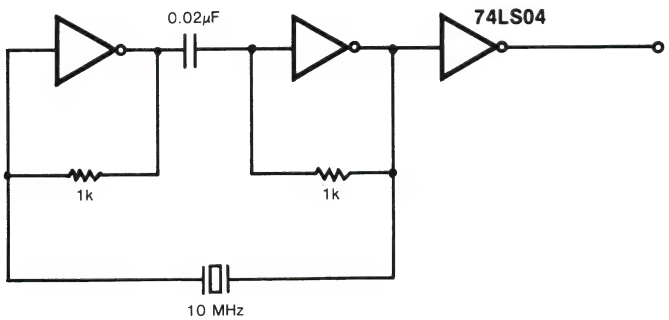
Crystal Clock Generator

(1) GD74LS00



Frequency (MHz)	C_1(pF)	C_2(pF)
1∼ 3	47	24
3∼ 4	47	22
4∼ 6	22	24
6∼ 8	22	22
8∼10	10	20
10∼13	0	20
13∼16	0	18

(2) GD74LS04



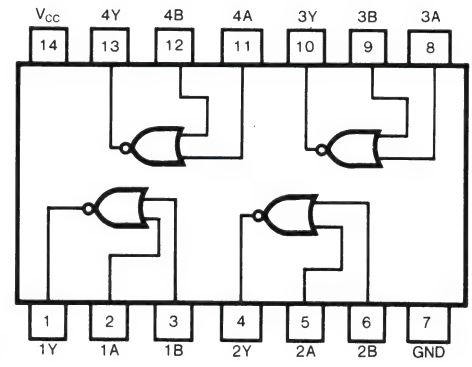
GD54/74LS02

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

Description

This device contains four independent 2-input NOR gates. It performs the Boolean functions $Y=\overline{A}\cdot\overline{B}$ or $Y=\overline{A+B}$ in positive logic.

Pin Configuration

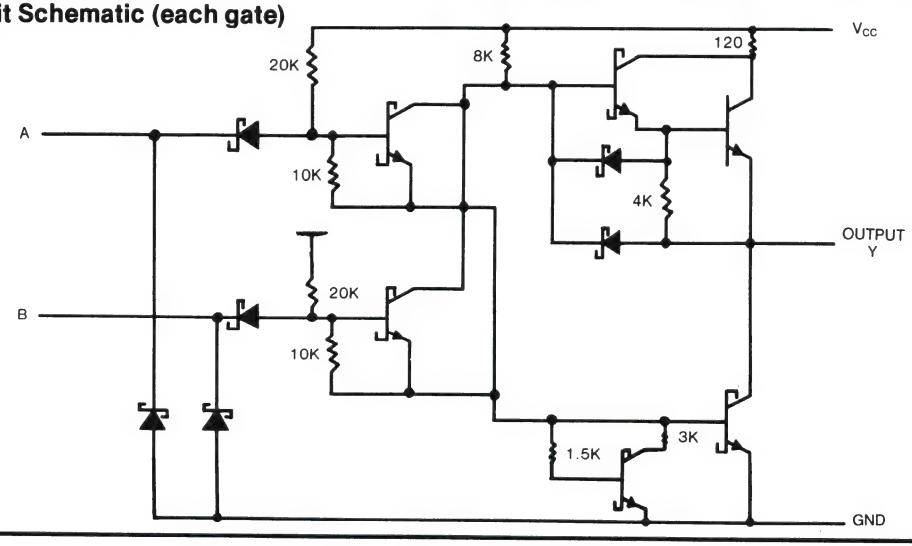


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

Circuit Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max, V_{IL}=Max		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max				1.6	3.2	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max				2.8	5.4	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	15	ns

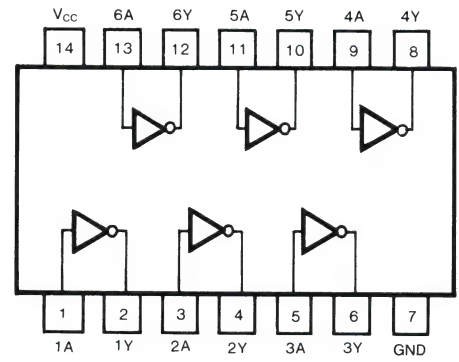
#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS04
HEX INVERTERS

Description

This device contains six independent inverters. It performs the Boolean function $Y=\overline{A}$.

Pin Configuration

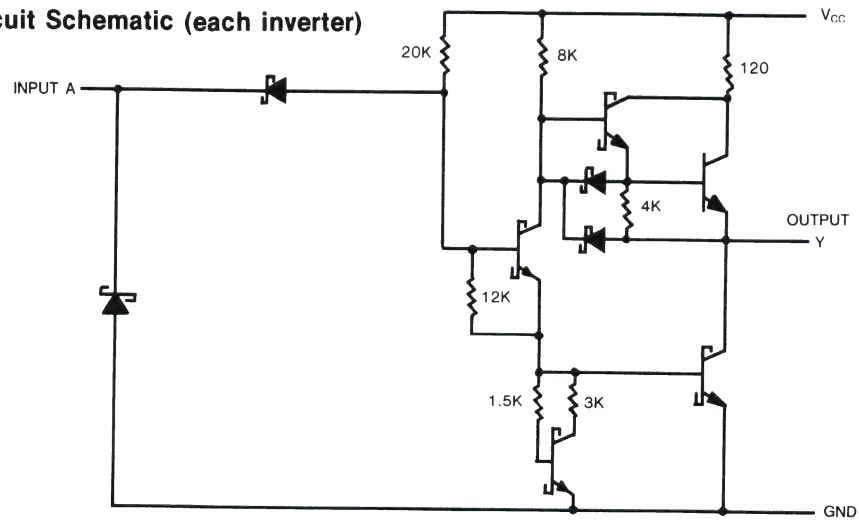


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

Circuit Schematic (each inverter)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
		I_{OH}=Max		74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
		V_{IH}=Min	I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max				1.2	2.4	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max				3.6	6.6	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	15	ns

#For load circuit and voltage waveforms, see page 3-11.

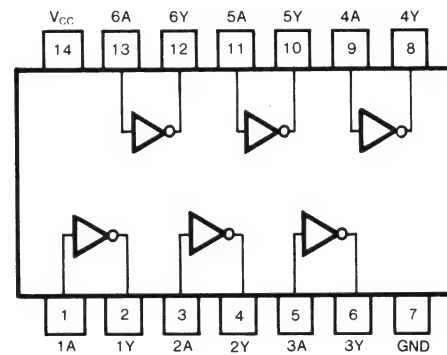
GD54/74LS05

HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

Description

This device contains six idenpendent inverts. It performs the Boolean function $Y=\overline{A}$. The open collector outputs require pull-up resistor to perform correctly. Open-collector devices are often used to generate higher V_{OH} levels.

Pin Configuration

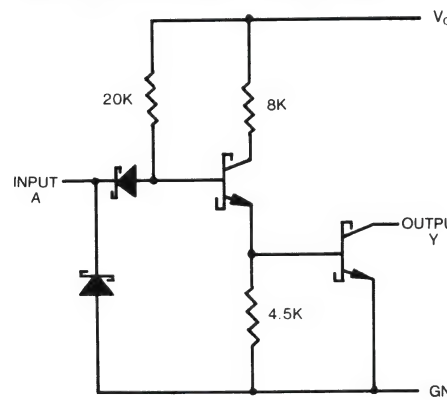


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

Circuit Schematic (each gate)



Pull-Up Resistor Equations

$$R_{MAX}=\frac{V_{CC}(Min)-V_{OH}}{N_1(I_{OH})+N_2(I_{IH})}$$

$$R_{MIN}=\frac{V_{CC}(Max)-V_{OL}}{I_{OL}-N_3(I_{IL})}$$

Where: $N_1(I_{OH})$=total maximum output high current for all outputs tied to pull-up resistor
$N_2(I_{IH})$=total maximum input high current for all inputs tied to pull-up resistor
$N_3(I_{IL})$=total maximum input low current for all inputs tied to pull-up resistor

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- output voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
V_{OH}	High-level output voltage	54,74			5.5	V
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage				54			0.7	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA					−1.5	V
I_{OH}	High-level output current		V_{CC}=Min, V_{IL}=Min, V_{OH}=Max					100	μA
V_{OL}	Low-level output voltage		V_{CC}=Min, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
				I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max				1.2	2.4	mA
I_{CCL}		Total with outputs low	V_{CC}=Max				3.6	6.6	mA

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		17	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	28	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS06

HEX INVERTED BUFFERS WITH OPEN-COLLECTOR OUTPUTS

Features

- High Output Voltage(30V)
- High Speed(t_{PD}=8.5nS typical)
- Low Power Dissipation(P_D=18mW per Gate)

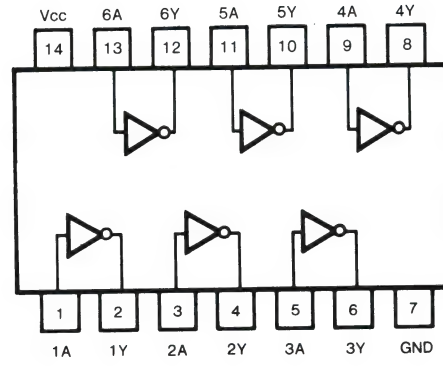
Description

This device contains hex inverted buffers with open-collector. It performs the Boolean function $Y=\overline{A}$ in positive Logic.

Function Table(each inverter)

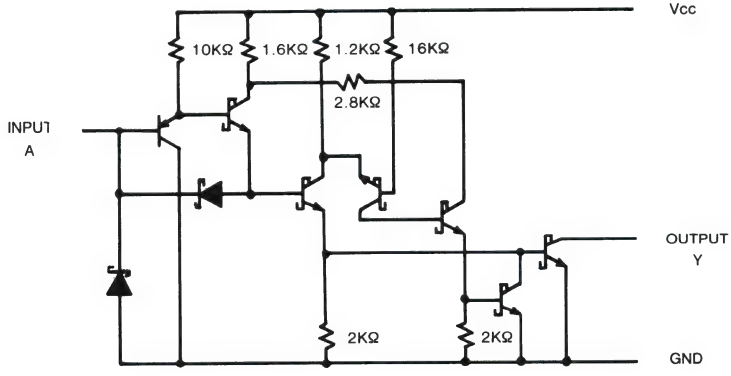
INPUT	OUTPUT
A	Y
H	L
L	H

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Circuit Schematic (each inverter)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Output voltage 30V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
V_{OH}	High-level output voltage	54,74			30	V
I_{OL}	Low-level output current	54			30	mA
		74			40	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.8	V
				74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−12mA				−1.5	V
I_{OH}	High-level output current		V_{CC}=Min, V_{IL}=Max, V_{OH}=Max				250	μA
V_{OL}	Low-level output voltage		V_{CC}=Min, V_{IH}=Min	I_{OL}=16mA			0.4	V
				I_{OL}=Max			0.7	
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V				20	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.4V				−0.2	mA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max			9	18	mA
I_{CCL}		Total with outputs low	V_{CC}=Max			35	60	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=110Ω		7	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	20	

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS07
HEX NON-INVERTED BUFFERS WITH OPEN-COLLECTOR OUTPUTS

Features

- High Output Voltage(30V)
- High Speed(t_{PD}=12 nS typical)
- Low Power Dissipation (P_D=13mW per Gate)

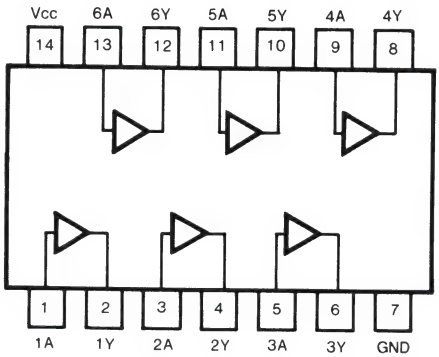
Description

This device contains hex non inverted buffers with open-collector. It performs the Boolean function Y=A in positive Logic.

Function Table(each inverter)

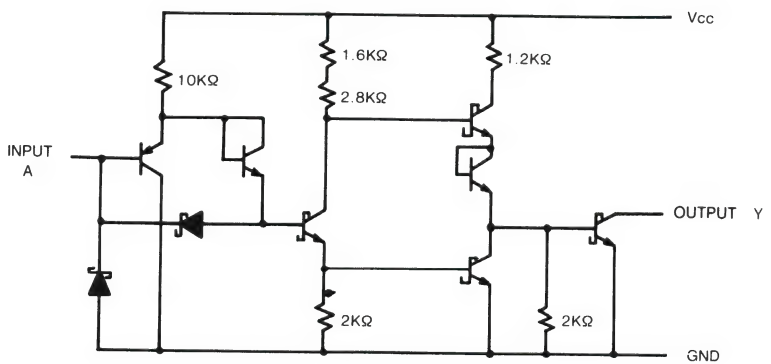
INPUT	OUTPUT
A	Y
H	H
L	L

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Circuit Schematics (each inverter)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 5.5V
- Output voltage 30V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
V_{OH}	High-level output voltage	54,74			30	V
I_{OL}	Low-level output current	54			30	mA
		74			40	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage				54			0.8	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−12mA					−1.5	V
I_{OH}	High-level output current		V_{CC}=Min, V_{IH}=Min, V_{OH}=Max					250	μA
V_{OL}	Low-level output voltage		V_{CC}=Min, V_{IL}=Max	I_{OL}=16mA				0.4	V
				I_{OL}=Max				0.7	
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=5.5V					1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.4V					−0.2	mA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max				7	14	mA
I_{CCL}		Total with outputs low	V_{CC}=Max				25	45	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=110Ω		6	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output			18	30	

#For load circuit and voltage waveforms, see page 3-11.

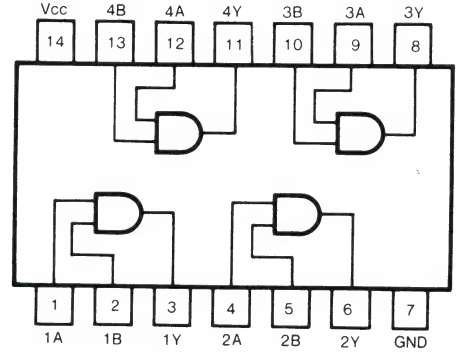
GD54/74LS08

QUADRUPLE 2-INPUT POSITIVE AND GATES

Description

This device contains four independent 2-input AND gates. It performs the Boolean functions $Y=A\cdot B$ or $Y=\overline{\overline{A}+\overline{B}}$ in positive logic.

Pin Configuration

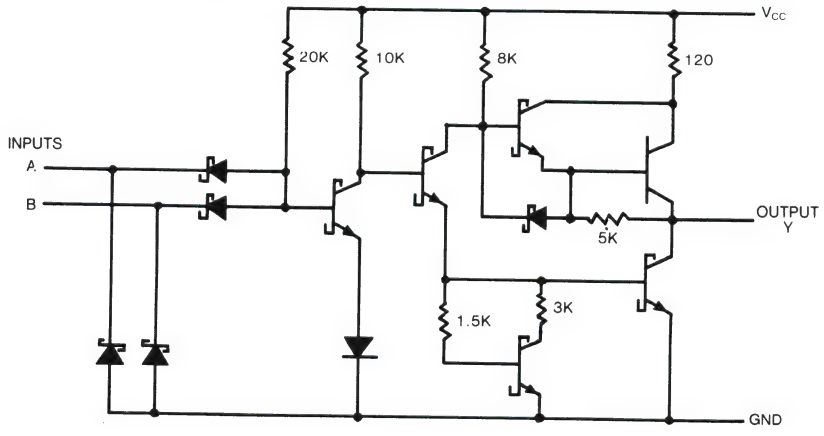


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

Circuit Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IH}=Min		54	2.5	3.4		V
		I_{OH}=Max		74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
		V_{IL}=Max	I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max				2.4	4.8	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max				4.4	8.8	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		8	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	20	ns

#For load circuit and voltage waveforms, see page 3-11.

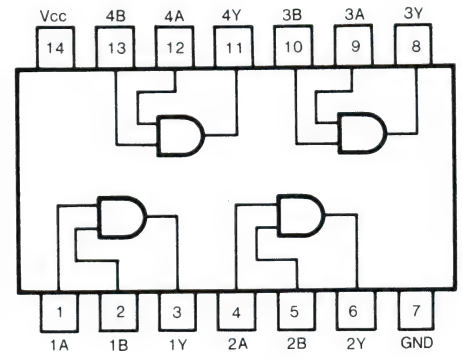
GD54/74LS09

QUADRUPLE 2-INPUT POSITIVE AND GATES WITH OPEN-COLLECTOR OUTPUTS

Description

This device contains four independent 2-input AND gates. It performs the Boolean functions $Y=A\cdot B$ or $Y=\overline{\overline{A}+\overline{B}}$ in positive logic. The open-collector outputs require pull up resistor to perform correctly. Open collector devices are often used to generate higher V_{OH} levels.

Pin Configuration

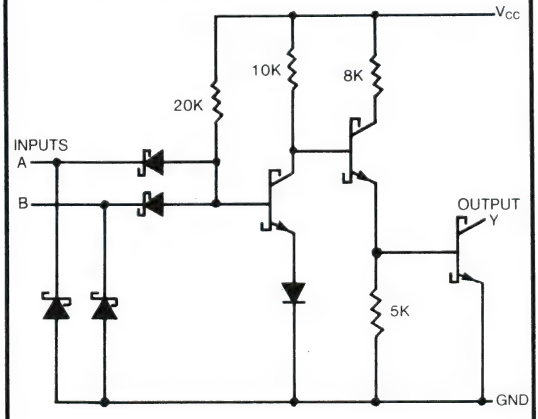


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

Circuit Schematic (each gate)



Pull-Up Resistor Equations

$$R_{MAX}=\frac{V_{CC}(Min)-V_{OH}}{N_1(I_{OH})+N_2(I_{IH})}$$

$$R_{MIN}=\frac{V_{CC}(Max)-V_{OL}}{I_{OL}-N_3(I_{IL})}$$

Where: $N_1(I_{OH})$=total maximum output high current for all outputs tied to pull-up resistor
$N_2(I_{IH})$=total maximum input high current for all inputs tied to pull-up resistor
$N_3(I_{IL})$=total maximum input low current for all inputs tied to pull-up resistor

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- output voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
V_{OH}	High-level output voltage	54,74			5.5	V
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
I_{OH}	High-level output current	V_{CC}=Min, V_{IH}=Min, V_{OH}=Max					100	μA
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max				2.4	4.8	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max				4.4	8.8	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			17	35	ns

#For load circuit and voltage waveforms, see page 3-11.

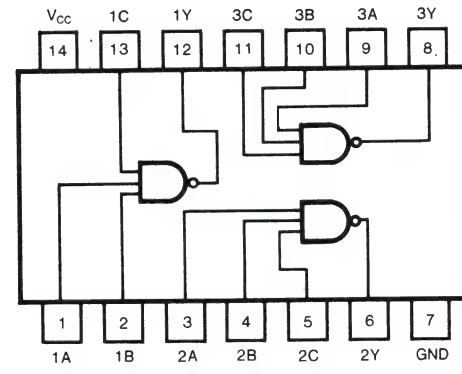
GD54/74LS10

TRIPLE 3-INPUT POSITIVE NAND GATES

Description

This device contains three independent 3-input NAND gates. It performs the Boolean functions $Y=\overline{A \cdot B \cdot C}$ or $Y=\overline{A}+\overline{B}+\overline{C}$ in positive logic.

Pin Configuration



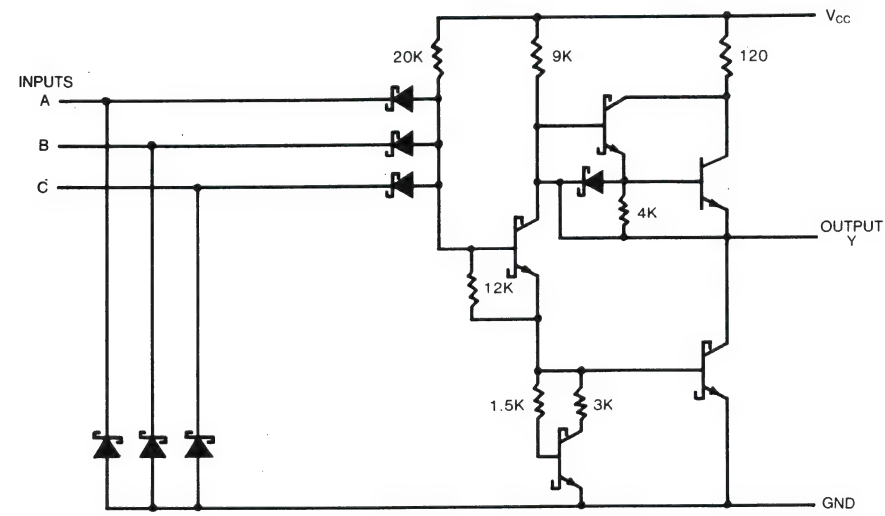
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each gate)

INPUTS		OUTPUT
A	N*	Y
L	L	H
H	L	H
L	H	H
H	H	L

* N=B·C

Circuit Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max,	V_{IL}=Max	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min	I_{OL}=4mA	74		0.25	0.4	V
		V_{IH}=Min	I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max				0.6	1.2	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max				1.8	3.3	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	15	ns

#For load circuit and voltage waveforms, see page 3-11.

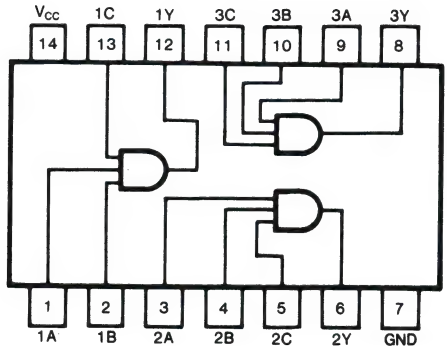
GD54/74LS11

TRIPLE 3-INPUT POSITIVE AND GATES

Description

This device contains three independent 3-input AND gates. It performs the Boolean functions $Y=A\cdot B\cdot C$ or $Y=\overline{A}+\overline{B}+\overline{C}$ in positive logic.

Pin Configuration



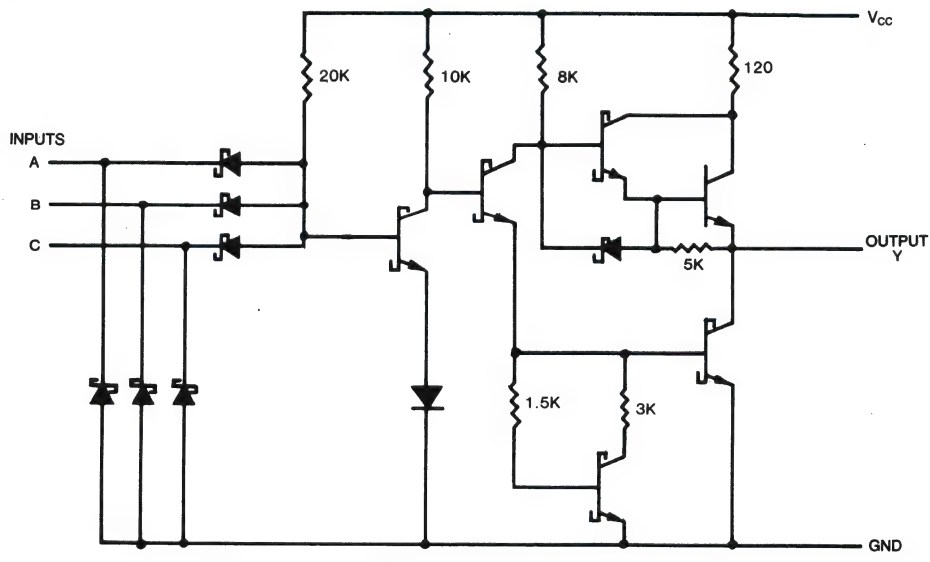
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each gate)

INPUTS		OUTPUT
A	N*	Y
L	L	L
H	L	L
L	H	L
H	H	H

* N=B·C

Circuit Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max				1.8	3.6	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max				3.3	6.6	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		8	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	20	ns

#For load circuit and voltage waveforms, see page 3-11.

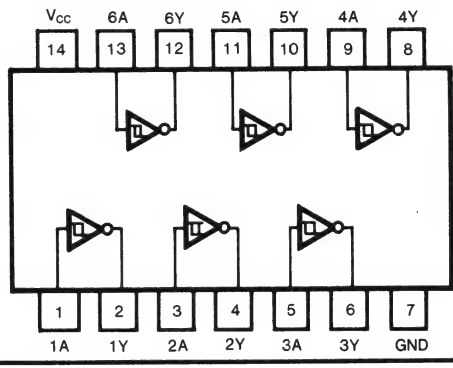
GD54/74LS14

HEX SCHMITT-TRIGGER INVERTERS

Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Pin Configuration

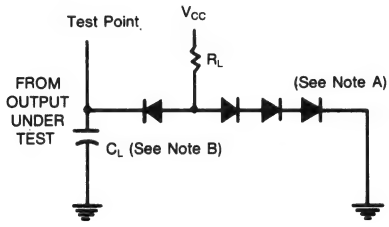


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

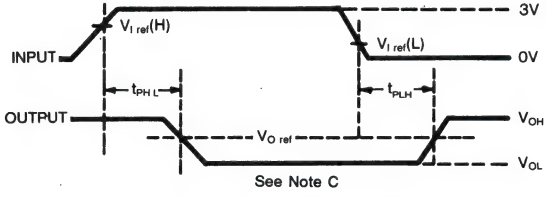
Function Table (each inverter)

INPUT	OUTPUT
A	Y
L	H
H	L

Parameter Measurement Information



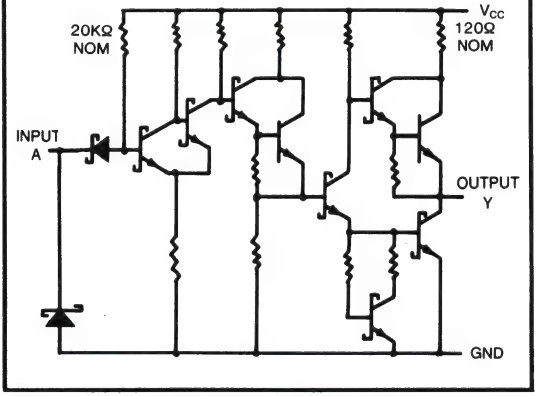
Load Circuit



VOLTAGE WAVEFORMS

Note: A. All diodes are IN916 or IN3064
B. C_L includes probe and jig capacitance

Circuit Schematics (each inverter)



Note C: Generator characteristics and reference voltage are

Generator Characteristics				Reference Voltage		
Z_{OUT}	PRR	tr	tf	V_I ref(H)	V_I ref(L)	V_O ref
50Ω	1MHz	15ns	6ns	1.6V	0.8V	1.3V

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)		V_{CC}=5V			1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)		V_{CC}=5V			0.5	0.8	1	V
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA					−1.5	V
$V_{T+}-V_{T-}$	Input Hysteresis (Note 1)		V_{CC}=5V			0.4	0.8		V
V_{OH}	High-level output voltage		V_{CC}=Min, I_{OH}=Max	V_I=V_{T-}Min	54	2.5	3.4		V
					74	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC}=Min, V_I=V_{T+}Max	I_{OL}=4mA	54,74		0.25	0.4	V
				I_{OL}=8mA	74		0.35	0.5	
I_{T+}	Input Current at Positive-Going Threshold		V_{CC}=5V, V_I=V_{T+}				−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold		V_{CC}=5V, V_I=V_{T-}				−0.18		mA
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max				8.6	16	mA
I_{CCL}		Total with outputs low	V_{CC}=Max				12	21	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Note more than one output should be shorted at a time, and the duration should not exceed one second.

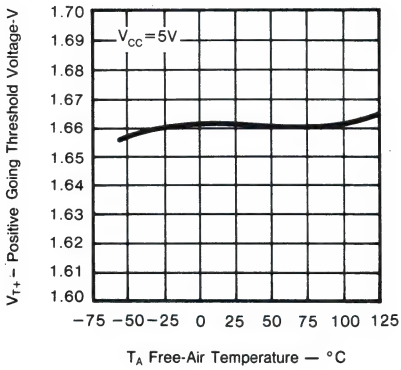
Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	22	ns

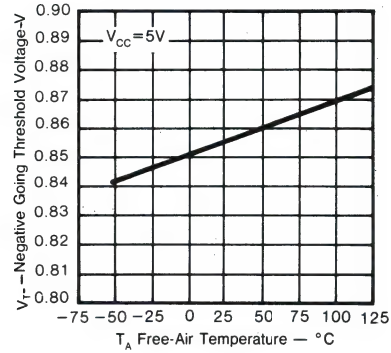
#For load circuit and voltage waveforms, see page 3-11.

Typical Characteristics

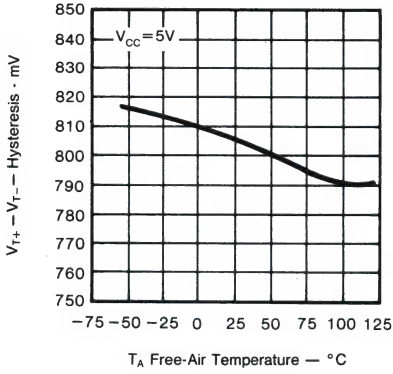
POSITIVE-GOING THRESHOLD VOLTAGE
V_S
FREE-AIR TEMPERATURE



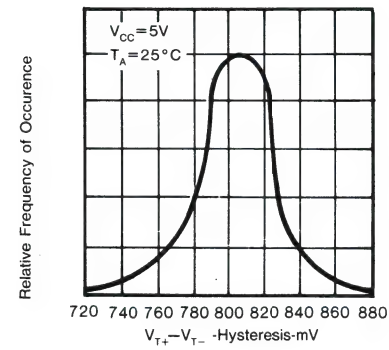
NEGATIVE-GOING THRESHOLD VOLTAGE
V_S
FREE-AIR TEMPERATURE



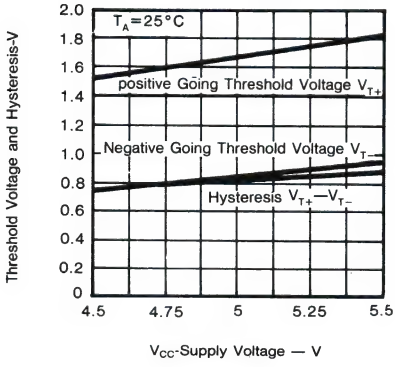
HYSTERESIS
V_S
FREE-AIR TEMPERATURE



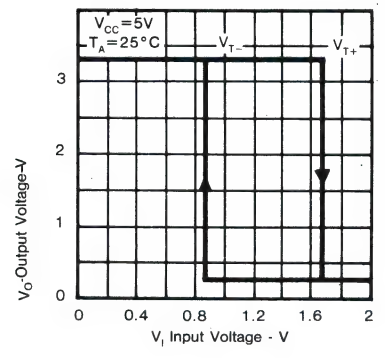
DISTRIBUTION OF UNIT
V_S
FOR HYSTERESIS



THRESHOLD VOLTAGE AND HYSTERESIS
V_S
SUPPLY VOLTAGE

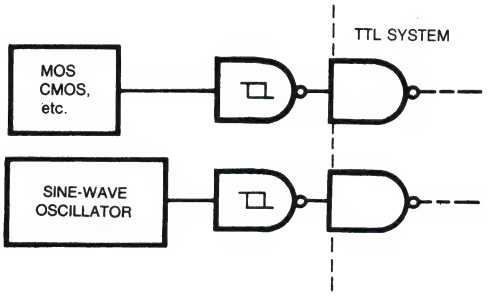


OUTPUT VOLTAGE
V_S
INPUT VOLTAGE

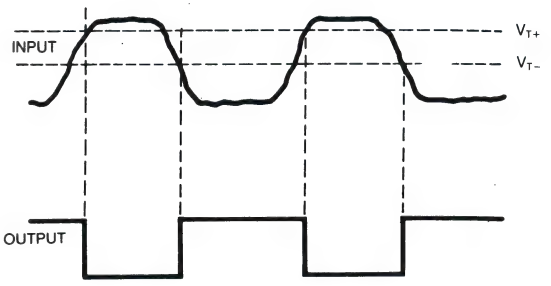


Typical Application Data

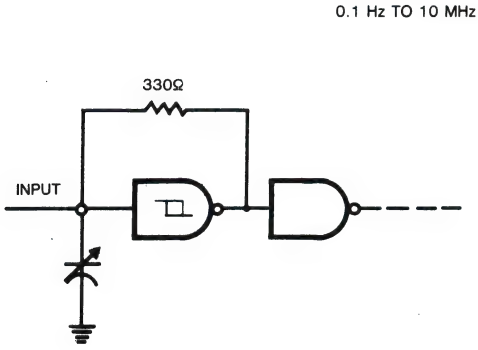
TYPICAL APPLICATION DATA



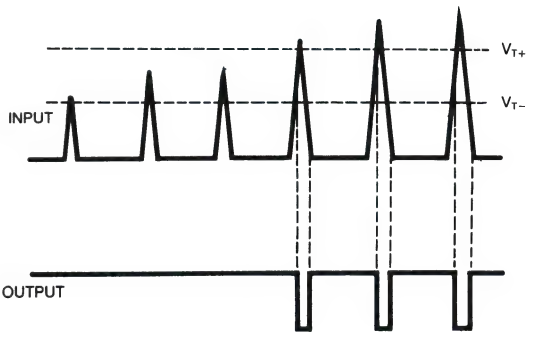
TTL SYSTEM INTERFACE
FOR SLOW INPUT WAVEFORMS



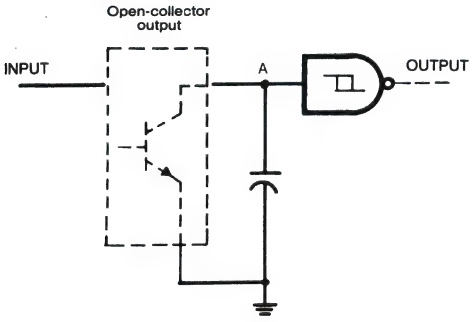
PULSE SHAPER

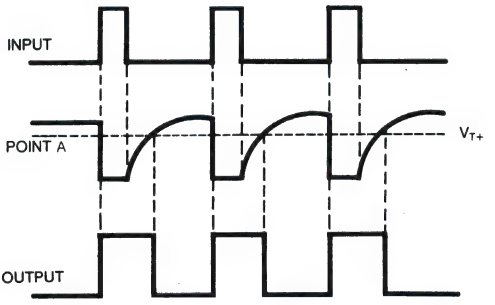


MULTIVIBRATOR



THRESHOLD DETECTOR





PULSE STRETCHER

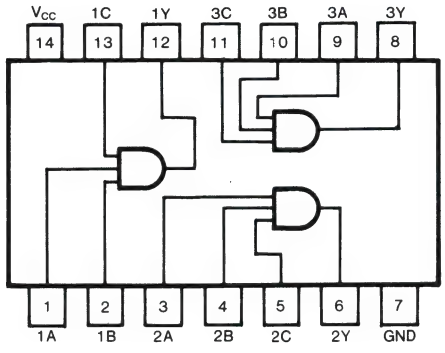
GD54/74LS15

TRIPLE 3-INPUT POSITIVE AND GATES WITH OPEN-COLLECTOR OUTPUTS

Description

This device contains three independent gates each of which performs the logic AND function. Y=ABC The open-collector outputs require external pull-up resistors for proper logical operation.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each gate)

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

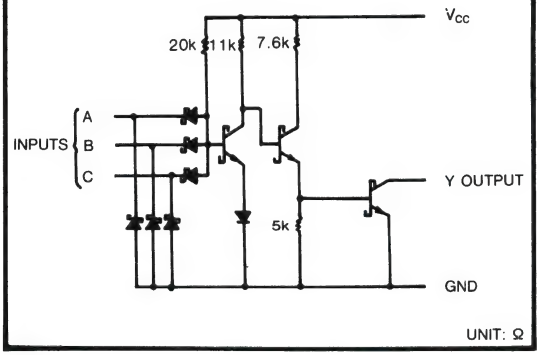
Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}(Min) - V_{OH}}{N_1(I_{OH}) + N_2(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}(Max) - V_{OL}}{I_{OL} - N_3(I_{IL})}$$

Where: N_1 (I_{OH})=total maximum output high current for all outputs tied to pull-up resistor
N_2 (I_{IH})=total maximum input high current for all inputs tied to pull-up resistor
N_3(I_{IL})=total maximum input low current for all inputs tied to pull-up resistor

Circuit Schematics (each gate)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Output voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
V_{OH}	High-level output voltage	54, 74			5.5	V
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
I_{OH}	High-level output current	V_{CC}=Min, V_{OH}=Max, V_{IH}=2V					100	μA
V_{OL}	Low-level output Voltage	V_{CC}=Min, V_{IL}=Max	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{CCH}	Supply curret — Total with outputs high	V_{CC}=Max				1.8	3.6	mA
I_{CCL}	Supply curret — Total with outputs low	V_{CC}=Max				3.3	6.6	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			17	35	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS16

HEX INVERTED BUFFERS WITH OPEN-COLLECTOR OUTPUTS

Features

- High Output Voltage (15V)
- High Speed (t_{PD}=8.5nS typical)
- Low Power Dissipation

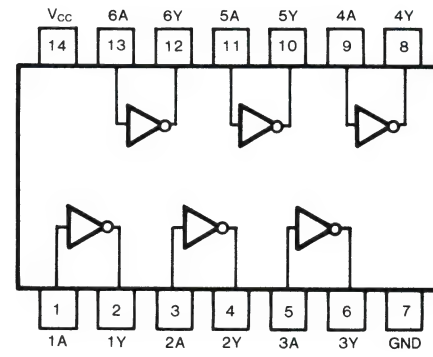
Description

This device contains hex inverted buffers with open collector. It performs the Boolean function $Y=\overline{A}$ in positive Logic.

Function Table (each inverter)

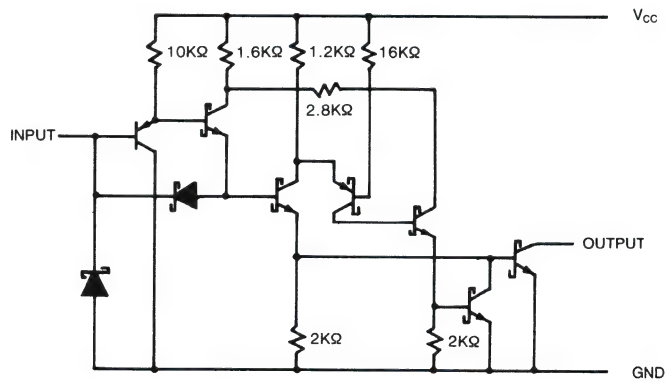
INPUT	OUTPUT
A	Y
H	L
L	H

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Circuit Schematics (each gate)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
V_{OH}	High-level output voltage	54, 74			15	V
I_{OL}	Low-level output current	54			30	mA
		74			40	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−12mA				−1.5	V
I_{OH}	High-level output current		V_{CC}=Min	V_{OH}=Max V_{IL}=Max			250	μA
V_{OL}	Low-level output voltage		V_{CC}=Min	I_{OL}=16mA			0.4	V
			V_{IH}=Min	I_{OL}=Max			0.7	
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V				20	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.4V				−0.2	mA
I_{CCH}	Supply curret	Total with outputs high	V_{CC}=Max			9	18	mA
I_{CCL}		Total with outputs low	V_{CC}=Max			35	60	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=110Ω		7	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	20	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS17
HEX NONINVERTED BUFFERS WITH OPEN-COLLECTOR OUTPUTS

Feature

- High Output Voltage (15V)
- High Speed (t_{PD}=9nS typical)
- Low Power Dissipation

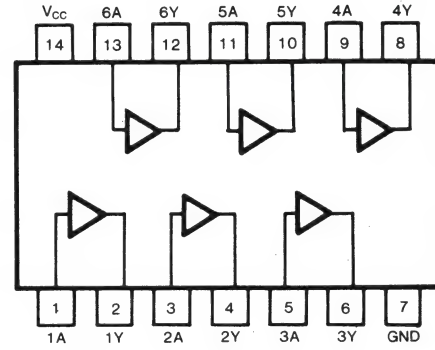
Description

This device contains hex noninverted buffers with open collector.
It performs the Boolean function Y=A in positive Logic.

Function Table

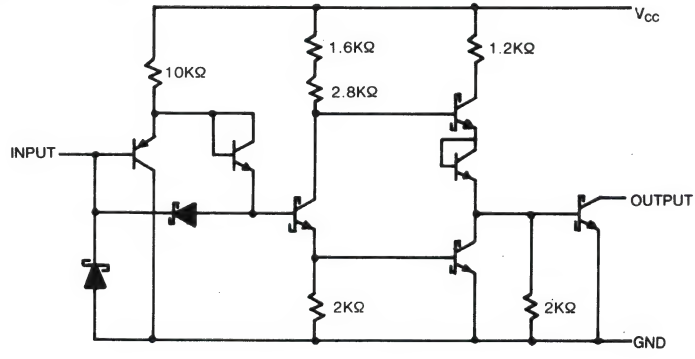
INPUT	OUTPUT
A	Y
H	H
L	L

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Circuit Schematics (each gate)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
V_{OH}	High-level output voltage	54, 74			15	V
I_{OL}	Low-level output current	54			30	mA
		74			40	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−12mA				−1.5	V
I_{OH}	High-level output current	V_{CC}=Min, V_{IH}=2.0V V_{OH}=15V				250	μA
V_{OL}	Low-level output voltage	V_{CC}=Min,	I_{OL}=16mA			0.4	V
		V_{IL}=Max,	I_{OL}= Max			0.7	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_{IH}=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_{IL}=0.4V				−0.2	mA
I_{CCH}	Supply current total with outputs high	V_{CC}=5.25V			7	14	mA
I_{CCL}	Supply current total with outputs low				25	45	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=110Ω		6	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output			18	30	ns

#For load circuit and voltage wave forms, see page 3-11.

GD54/74LS20

DUAL 4-INPUT POSITIVE NAND GATES

Description

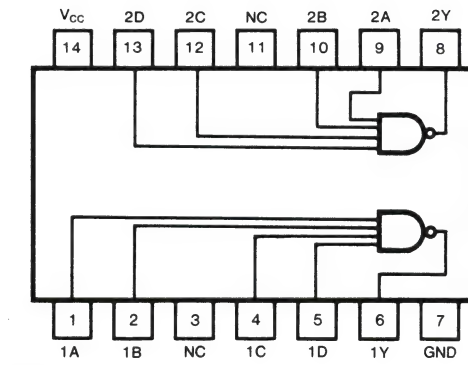
This device contains two independent 4-input NAND gates. It performs the Boolean functions $Y=\overline{A \cdot B \cdot C \cdot D}$ or $Y=\overline{A}+\overline{B}+\overline{C}+\overline{D}$ in positive logic.

Function Table (each gate)

INPUTS		OUTPUT
A	N*	Y
L	L	H
H	L	H
L	H	H
H	H	L

* N=B·C·D

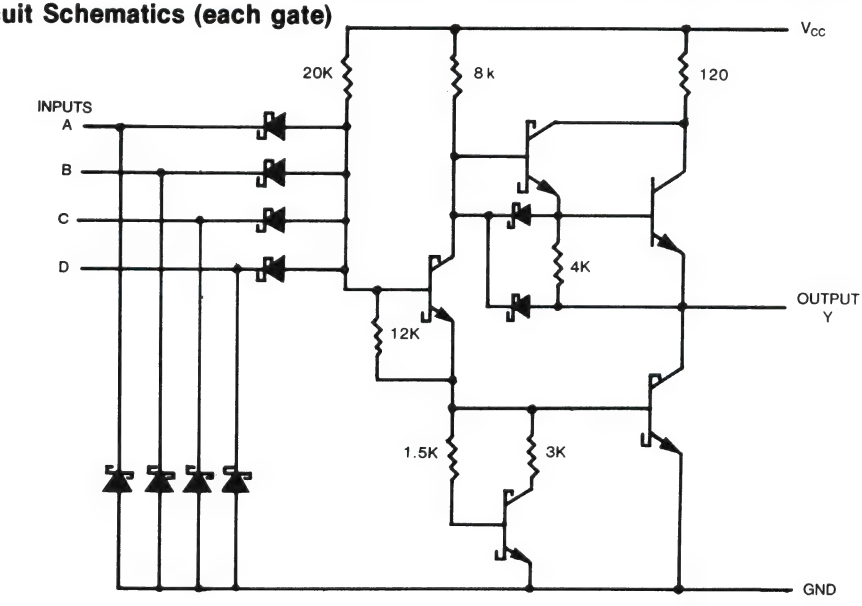
Pin Configuration



NC: No internal connection

Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Circuit Schematics (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
		V_{IH}=Min	I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max				0.4	0.8	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max				1.2	2.2	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	15	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS21

DUAL 4-INPUT POSITIVE AND GATES

Description

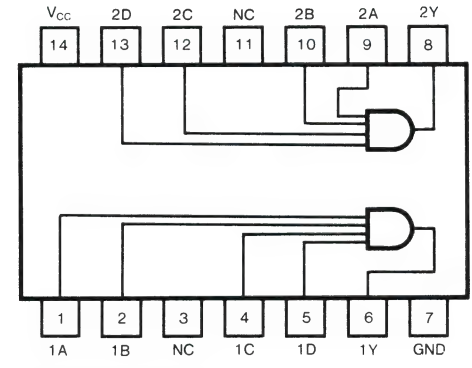
This device contains two independent 4-input AND gates. It performs the Boolean functions $Y=A\cdot B\cdot C\cdot D$ or $Y=\overline{A}+\overline{B}+\overline{C}+\overline{D}$ in positive logic.

Function Table (each gate)

INPUTS		OUTPUT
A	N*	Y
L	L	L
H	L	L
L	H	L
H	H	H

* N=B·C·D

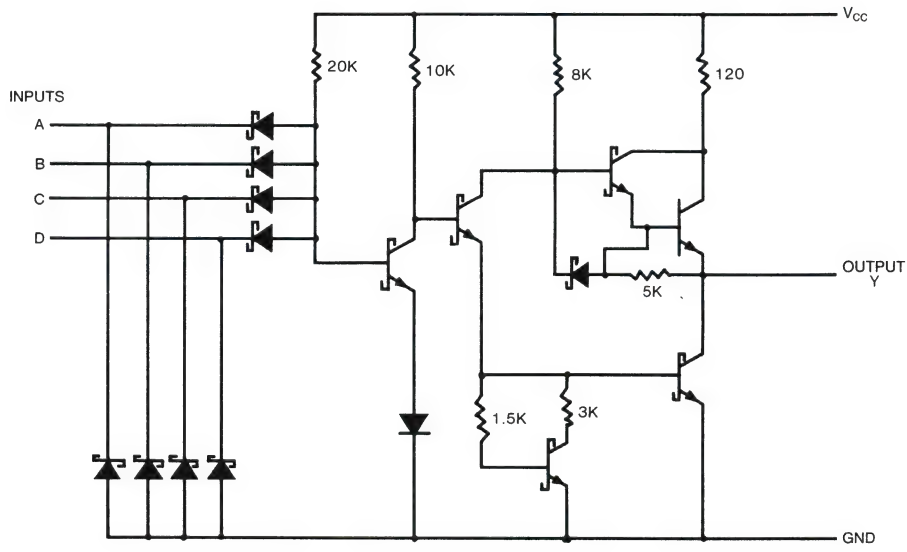
Pin Configuration



NC: No internal connection

Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Circuit Schematics (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max,	V_{IH}= Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
		V_{IL}=Max	I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max				1.2	2.4	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max				2.2	4.4	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		8	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	20	ns

#For load circuit and voltage wave forms, see page 3-11.

GD54/74LS26
QUAD 2-INPUT NAND GATES WITH HIGH VOLTAGE OPEN-COLLECTOR OUTPUTS

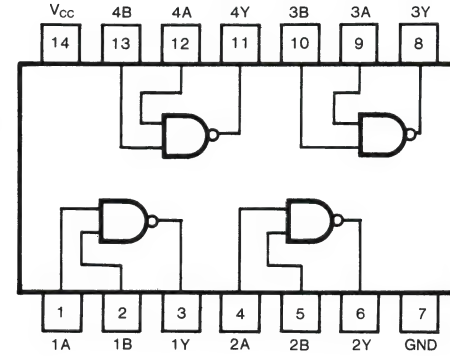
Features

- Usable in AND-Tie connection
- High Output Voltage (15V)

Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pin Configuration



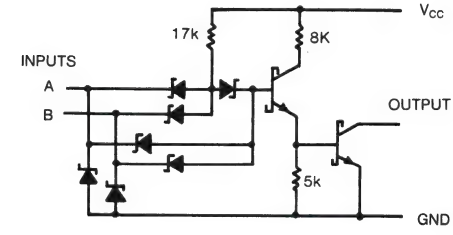
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each gate)

$Y=\overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

Circuit Schematics (each gate)



Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}(Min) - V_{OH}}{N_1(I_{OH}) + N_2(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}(Max) - V_{OL}}{I_{OL} - N_3(I_{IL})}$$

Where: $N_1(I_{OH})$=total maximum output high current for all outputs tied to pull-up resistor
N_2 (I_{IH})=total maximum input high current for all inputs tied to pull-up resistor
$N_3(I_{IL})$=total maximum input low current for all inputs tied to pull-up resistor

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Output voltage 15V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
V_{OH}	High-level output voltage	54, 74			15	V
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−12mA				−1.5	V
I_{OH}	High-level output current	V_{CC}=Min, V_{IL}=Max	V_{OH}=12V			50	μA
			V_{OH}=15V			1000	
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max,	I_{OL}=4mA		0.25	0.4	V
			I_{OL}= Max		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_{IH}=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_{IL}=0.4V				−0.4	mA
I_{CCH}	Supply current total with outputs high	V_{CC}=5.25V			0.8	1.6	mA
I_{CCL}	Supply current total with outputs low				2.4	4.4	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		17	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	28	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS27

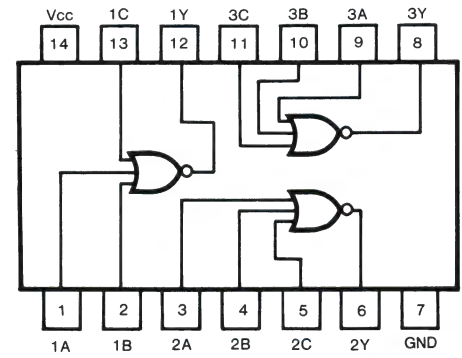
TRIPLE 3-INPUT POSITIVE-NOR GATES

Description

This device contains three independent gates each of which performs the logic NOR function.

; $Y=\overline{A+B+C}$

Pin Configuration



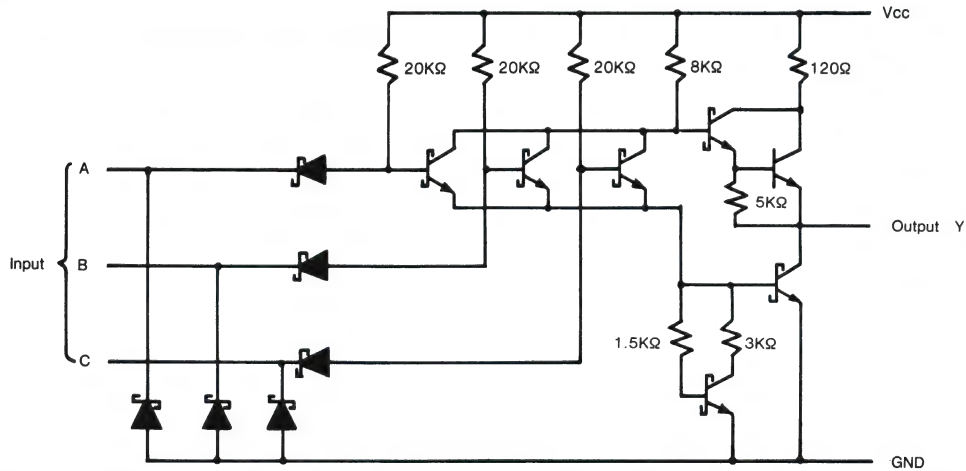
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table(each gate)

Input		Output
A	N*	Y
L	L	H
L	H	L
H	L	L
H	H	L

*N=B+C

Circuit Schematics (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max,		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
		V_{IH}=Min	I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max			2	4	mA
I_{CCL}		Total with outputs low	V_{CC}=Max			3.4	6.8	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2KΩ		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	15	

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS30

8-INPUT POSITIVE NAND GATE

Description

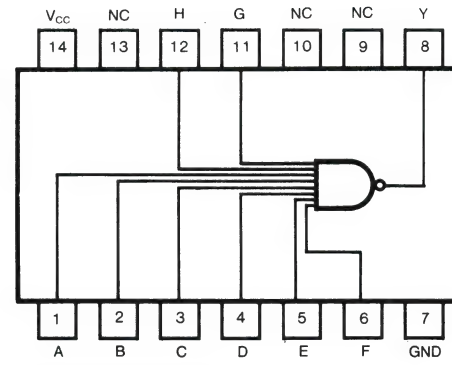
This device contains a single 8-input NAND gate and performs the following Boolean functions in positive logic.

$Y=\overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$ or
$Y=\overline{A}+\overline{B}+\overline{C}+\overline{D}+\overline{E}+\overline{F}+\overline{G}+\overline{H}$

Function Table

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

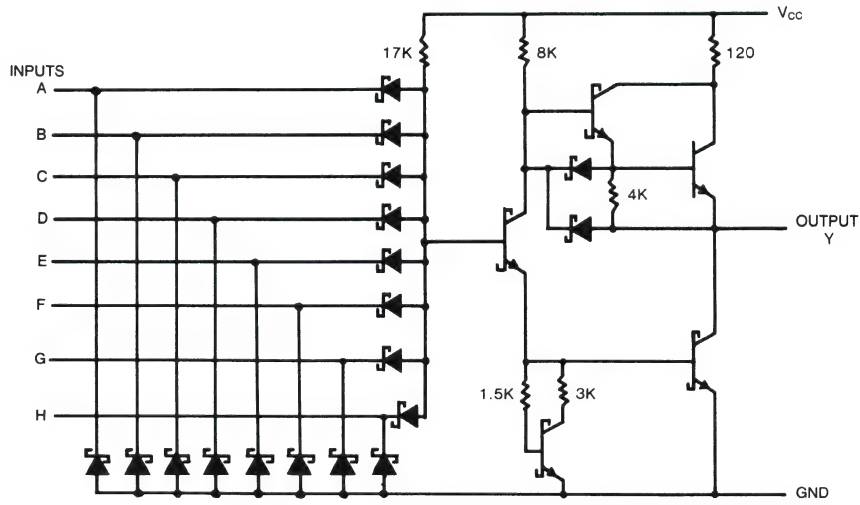
Pin Configuration



NC: No internal connection

Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Circuit Schematics (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max,	V_{IL}=Max	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
		V_{IH}=Min	I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max				0.36	0.5	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max				0.6	1.1	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time low-to-high-level output,	C_L=15pF, R_L=2kΩ		8	15	ns
t_{PHL}	Propagation delay time high-to-low-level output,			13	20	ns

#For load circuit and voltage wave forms, see page 3-11.

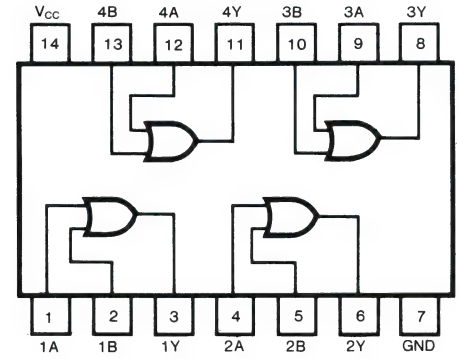
GD54/74LS32

QUADRUPLE 2-INPUT POSITIVE OR GATES

Description

This device contains four independent 2-input OR gates. It performs the Boolean functions $Y=\overline{\overline{A}\cdot\overline{B}}$ or $Y=A+B$ in positive logic.

Pin Configuration

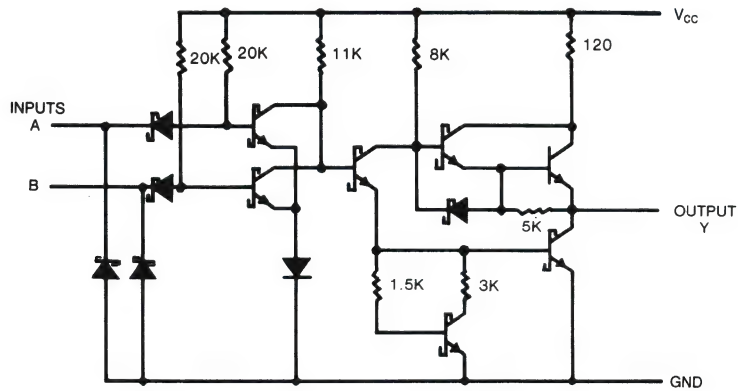


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

Circuit Schematics (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
		V_{IL}=Max	I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max				3.1	6.2	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max				4.9	9.8	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output			14	22	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS38
QUAD 2-INPUT NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

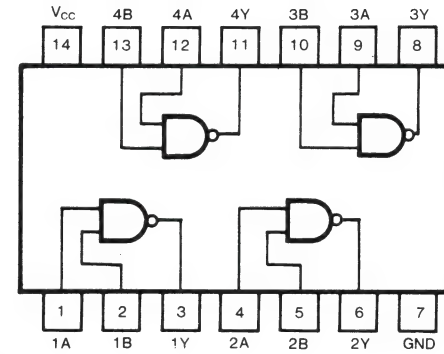
Features

- Usable in AND-Tie connection
- High fan-out (I_{OL}=24mA max)

Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each gate)

$Y=\overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

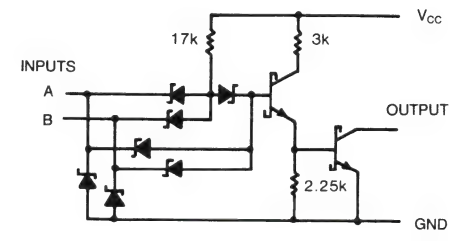
Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}(Min)-V_{OH}}{N_1(I_{OH})+N_2(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}(Max)-V_{OL}}{I_{OL}-N_3(I_{IL})}$$

Where: $N_1(I_{OH})$=total maximum output high current for all outputs tied to pull-up resistor
N_2 (I_{IH})=total maximum input high current for all inputs tied to pull-up resistor
$N_3(I_{IL})$=total maximum input low current for all inputs tied to pull-up resistor

Circuit Schematics (each gate)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Output voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
V_{OH}	High-level output voltage	54, 74			5.5	V
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage				54			0.7	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA					−1.5	V
I_{OH}	High-level output current		V_{CC}=Min, V_{OH}=Max, V_{IL}=Max					250	μA
V_{OL}	Low-level output voltage		V_{CC}=Min, V_{IH}=Min	I_{OL}=12mA	54, 74		0.25	0.4	V
				I_{OL}=24mA	74		0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{CCH}	Supply curret	Total with outputs high	V_{CC}=Max				0.9	2	mA
I_{CCL}		Total with outputs low	V_{CC}=Max				6	12	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=45pF, R_L=667Ω		20	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output			18	28	ns

#For load circuit and voltage waveforms, see page 3-11.

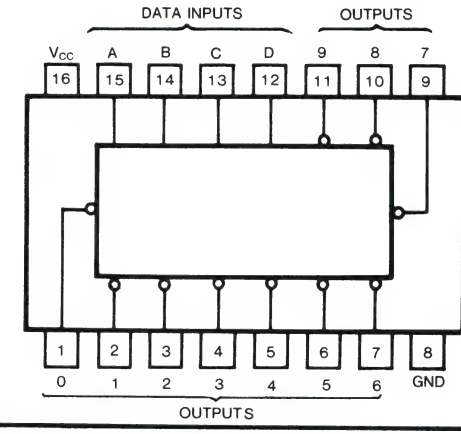
GD54/74LS42

BCD/DECIMAL DECODERS

Features

- Diode clamped inputs
- Also for application as 4-line-to-16-line decoders; 3-line-to-8-line decoders
- All outputs are high for invalid input conditions
- Usable as a 3-bit binary/octal decoders

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

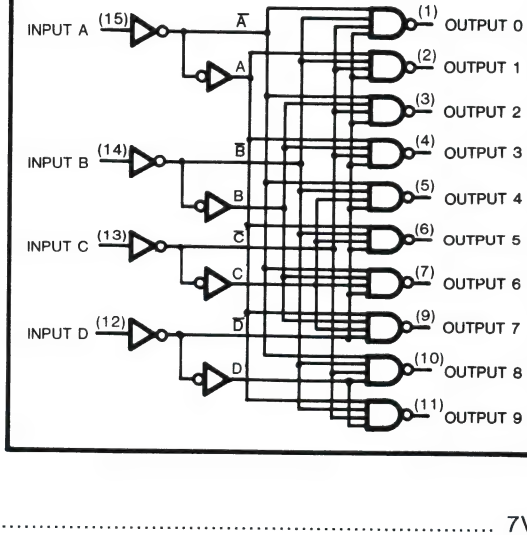
Description

These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid (10-15) input conditions.

Function Table

No.	BCD Input				Decimal Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54, 74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				7	13	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with all outputs open, and all inputs grounded.

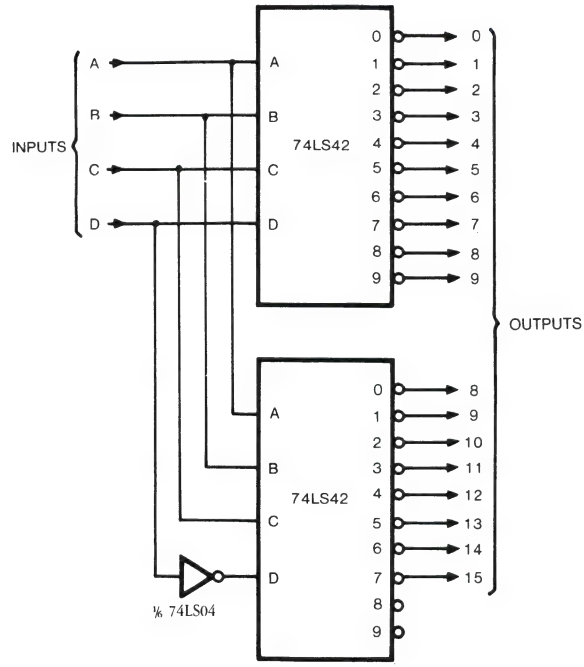
Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL*	FROM (INPUT)	TO (OUTUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Data	2 Levels of Logic	C_L=15pF, R_L=2kΩ		15	25	ns
t_{PHL}					15	25	
t_{PLH}	Data	3 Levels of Logic			20	30	ns
t_{PHL}					20	30	

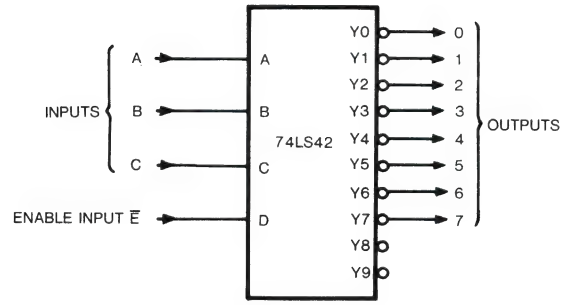
* t_{PLH}=Propagation delay time, low-to-high-level output
* t_{PHL}=Propagation delay time, high-to-low-level output

APPLICATION EXAMPLES

(1) 4-bit binary/hexadecimal decoder



(2) 3-bit binary/octal decoder with enable input



GD54/74LS51

AND-OR-INVERT GATES

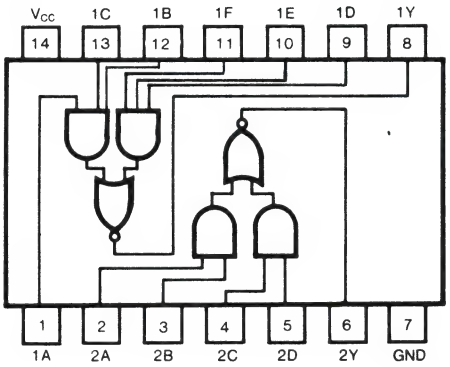
Description

This device contains a NOR gate with two 2-input AND gates as the inputs and a NOR gate with two 3-input AND gates as the inputs.

It performs the following Boolean functions;

$$1Y=\overline{1A\cdot 1B\cdot 1C + 1D\cdot 1E\cdot 1F}$$
$$2Y=\overline{2A\cdot 2B + 2C\cdot 2D}$$

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

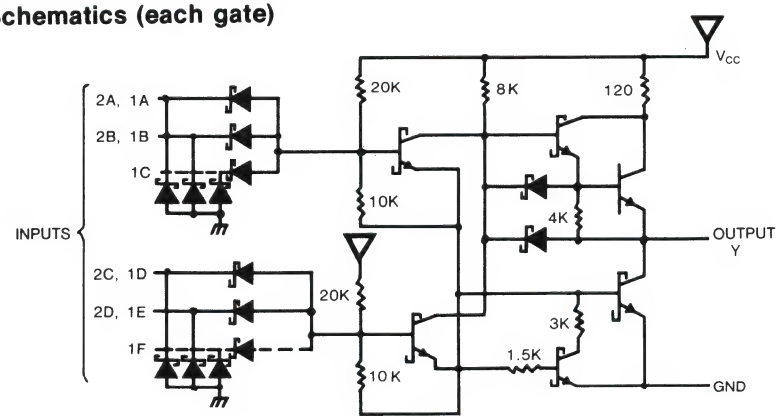
N*	M*	1Y
L	L	H
H	L	L
L	H	L
H	H	L

*N=1A·1B·1C
*M=1D·1E·1F

N*	M*	1Y
L	L	H
H	L	L
L	H	L
H	H	L

*N=2A·2B
*M=2C·2D

Circuit Schematics (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IH}=Max	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
		V_{IH}=Min	I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max				0.8	1.6	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max				1.4	2.8	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12.5	20	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS55

2WIDE 4-INPUT AND-OR-INVERT GATES

Description

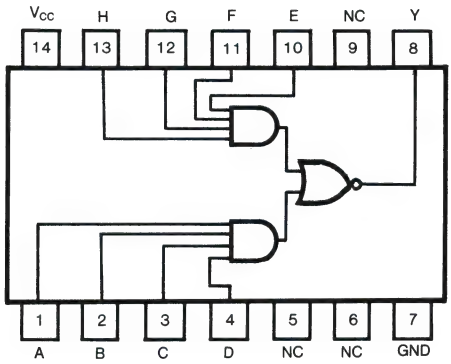
This device contains a combination of gates each of which performs the logic AND-OR-INVERT function.

$Y=\overline{ABCD+EFGH}$

Function Table

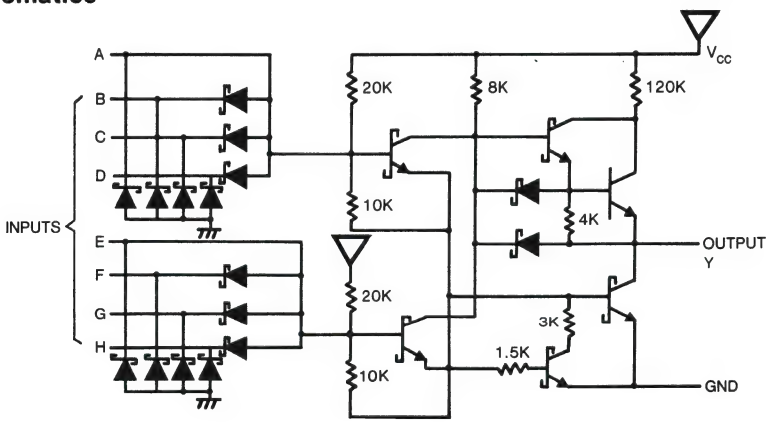
Inputs								Output
A	B	C	D	E	F	G	H	Y
H	H	H	H	X	X	X	X	L
X	X	X	X	H	H	H	H	L
All other combinations								H

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Circuit Schematics



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54S ..... −55° to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IH}=Min, V_{IL}=Max	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	μA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max				0.4	0.8	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max				0.7	1.3	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed ond second.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12.5	20	ns

#For load circuit and voltage waveforms, see page 3-11.

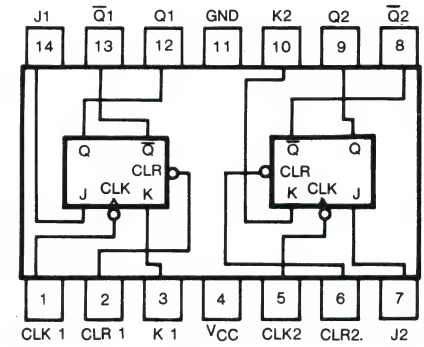
GD54/74LS73A

DUAL NEGATIVE EDGE-TRIGGERED MASTER-SALVE J-K FLIP-FLOPS WITH CLEAR AND COMPLEMENTARY OUTPUTS

Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J and K inputs is allowed to change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the levels of the other inputs.

Pin Configuration



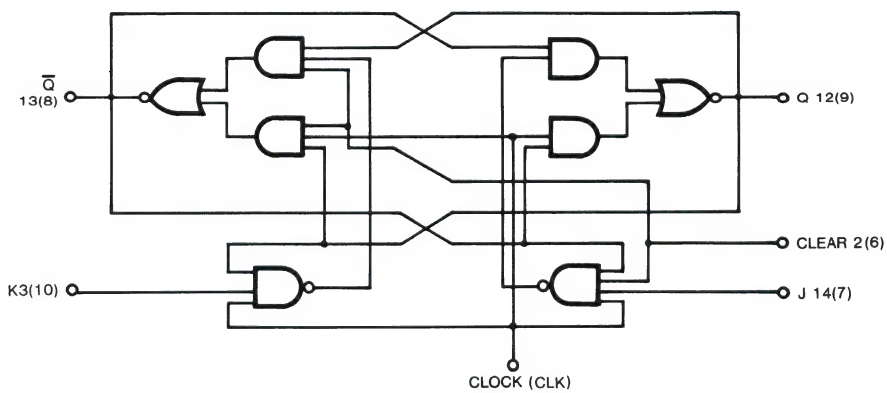
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table(each gate)

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_o	$\overline{Q}_o$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_o	$\overline{Q}_o$

X= Either Low or High Logic Level
↓=Negative going edge of pulse
Q_o=The output logic level before the indicated input conditions were established.
Toggle=Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Logic Diagram (Each Flip-Flop)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output Current		54, 74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{clock}	Clock frequency			0		30	MHz
t_w	Pluse width	Clock high		20			ns
		Preset low		25			
		Clear low		25			
t_{su}	Clear inactive-state setup time			20↓			ns
t_h	Data hold time			0↓			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage				54			0.7	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18 mA					−1.5	V
V_{OH}	High-level output voltage		V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
			I_{OH}=Max, V_{IH}=Min		74	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
				I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	J,K	V_{CC}=5.25V, V_I=7V					0.1	mA
		Clear						0.3	
		Clock						0.4	
I_{IH}	High-level input current	J,K	V_{CC}=5.25V, V_I=2.7V					20	μA
		Clear						60	
		Clock						80	
I_{IL}	Low-level input current	J,K	V_{CC}=5.25V, V_I=0.4V					−0.4	mA
		Clear						−0.8	
		Clock						−0.8	
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current		V_{CC}=Max (Note 3)				4	6	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

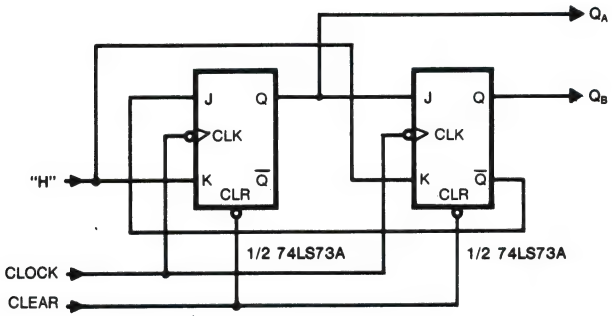
SYMBOL*	FROM(INPUT)	TO(OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}			$C_L=15$ pF $R_L=2K\Omega$	30	45		MHz
t_{PLH}	Clear, Clock	Q or $\overline{Q}$			15	20	ns
t_{PHL}					15	20	

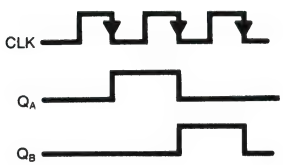
* f_{max}=maximum clock frequency
* t_{PLH}=propagation delay time, low-to-high-level output.
* t_{PHL}=propagation delay time, high-to-low-level output.

#For load circuit and voltage waveforms, see page 3-11.

Application Example

HIGH-SPEED 1/3 DIVIDER





GD54/74LS74A

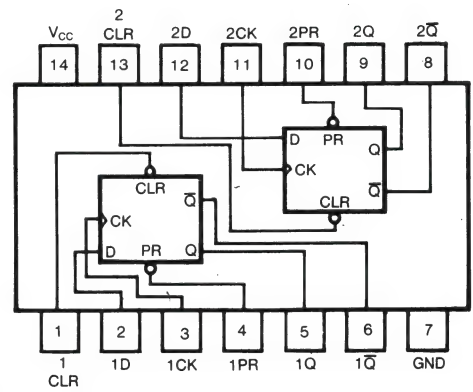
DUAL D-TYPE POSITIVE EDGE-TRIGGERD FLIP-FLOPS WITH PRESET AND CLEAR

Description

This device contains two independent D-type positive edge triggered flip-flops.

A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triger-ing occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

Pin Configuration



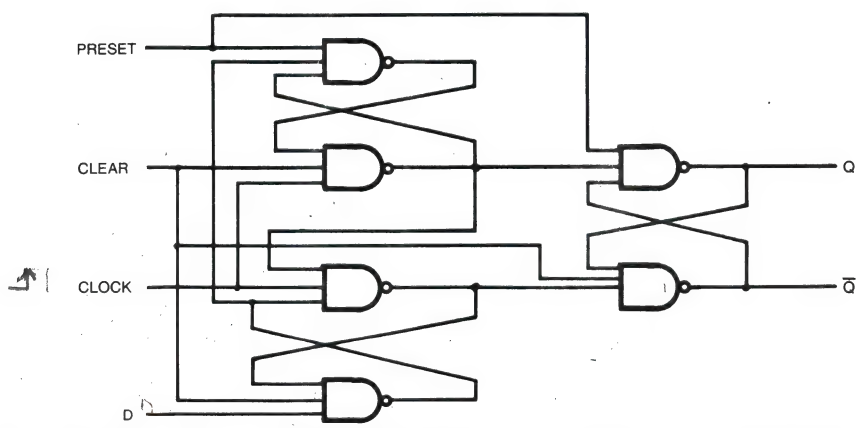
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum, Furthermore, this configuration is nonstable; that is it will not persist when either preset or clear returns to its inactive (high) level.

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_O	$\overline{Q}_O$

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54,74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{clock}	Clock frequency			0		25	MHz
t_w	Pulse width	Clock high		25			ns
		Preset or clear low		25			
t_{SU}	Setup time	high-level data		20↑*			ns
		low-level data		20↑*			
t_h	Hold time			5↑*			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

* ↑ for rising edge

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
		I_{OH}=Max, V_{IH}=Min		75	2.7	3.4		
V_{OL}	Low level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	D, CK				0.1	mA
			PR, CLR				0.2	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	D, CK				20	μA
			PR, CLR				40	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	D, CK				−0.4	mA
			PR, CLR				−0.8	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				4	8	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

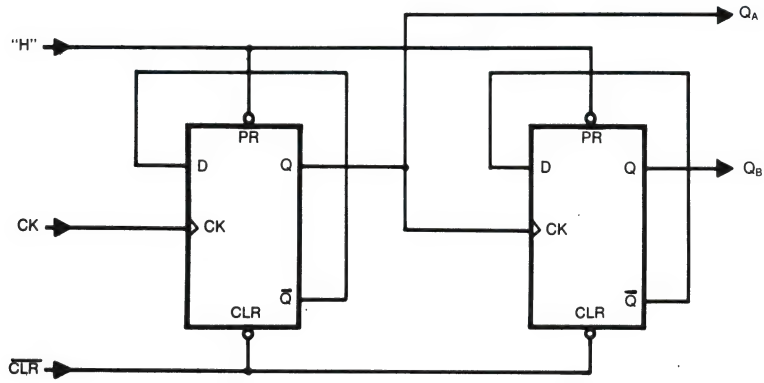
Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

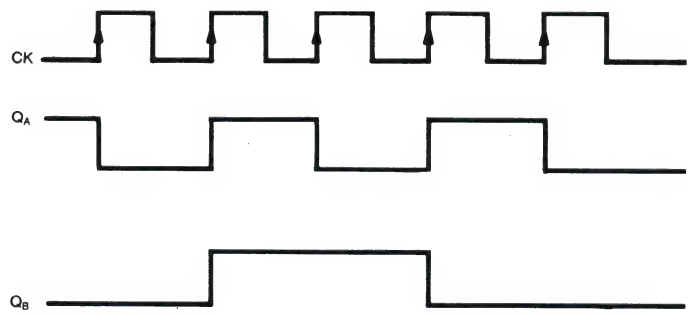
SYMBOL*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}			$C_L=15pF$	25	33		MHz
t_{PLH}	Clear, preset or Clock (as appropriate)	Q or $\overline{Q}$	$R_L=2K\Omega$		13	25	ns
t_{PHL}					25	40	

* f_{max}=maximum clock frequency
* t_{PLH}=propagation delay time, low-to-high-level output.
* t_{PHL}=propagation delay time, high-to-low-level output.

#For load circuit and voltage waveforms, see page 3-11.

Application Example
¼ divider





#For load circuit and voltage waveforms, see page 3-12.

GD54/74LS75

4-BIT BISTABLE LATCH

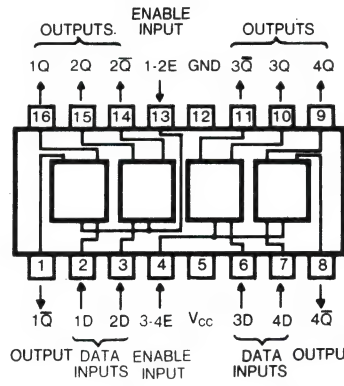
Features

- Enable inputs common to two circuits each
- Q ad $\overline{Q}$ outputs

Description

This device contains 4 D-type latch circuits and is provided with enable inputs E common to 2 circuits each. When E is high, the information from the data input D appears in the outputs Q and $\overline{Q}$. When the D signal changes, the signal that appears in outputs Q and $\overline{Q}$ also changes. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of Q and $\overline{Q}$ does not change even if D is changed.

Pin Configuration



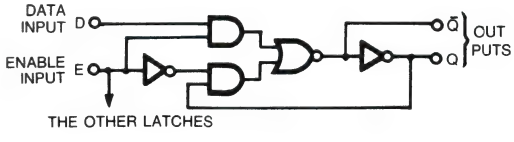
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (Note 1)

E	D	Q	$\overline{Q}$
H	H	H	L
H	L	L	H
L	X	Q^0	$\overline{Q}^0$

Note 1. Q^0,$\overline{Q}^0$: Level of Q and $\overline{Q}$ before the indicated steady-state input conditions were established.
X : Irrelevant

Block Diagram (Each Latch)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
t_W	Width of enable pulse		20			ns
t_{SU}	Set up time		20			ns
t_h	Hold time		5			ns
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output Voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max, V_{IH}=Min	54	2.5	3.5		V
				74	2.7	3.5		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	D				0.1	mA
			E				0.4	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	D				20	μA
			E				80	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	D				−0.4	mA
			E				−1.6	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				6.3	12	mA

Note 1: All typicals are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with all outputs open and all inputs grounded

Switching Characteristics, V_{CC}=5V, T_A=25°, unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D to output Q	C_L=15pF, R_L=2kΩ		15	27	ns
t_{PHL}				9	17	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D to output $\overline{Q}$			12	20	ns
t_{PHL}				7	15	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation Time, from input E to output Q			15	27	ns
t_{PHL}				14	25	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E to output $\overline{Q}$			16	30	ns
t_{PHL}				7	15	ns

GD54/74LS85

4-BIT MAGNITUDE COMPARATORS

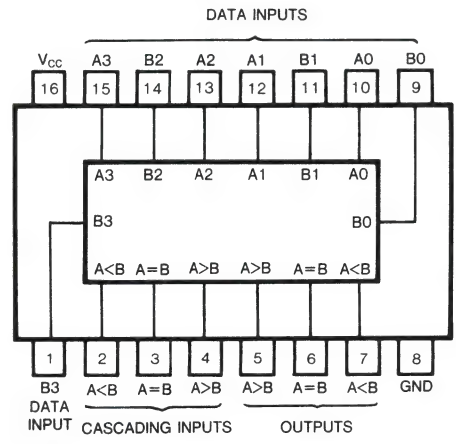
Features

- Typical power dissipation 52 mW
- Typical delay (4-bit words) 24 ns

Description

These four-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A>B, A<B, and A=B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A=B input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

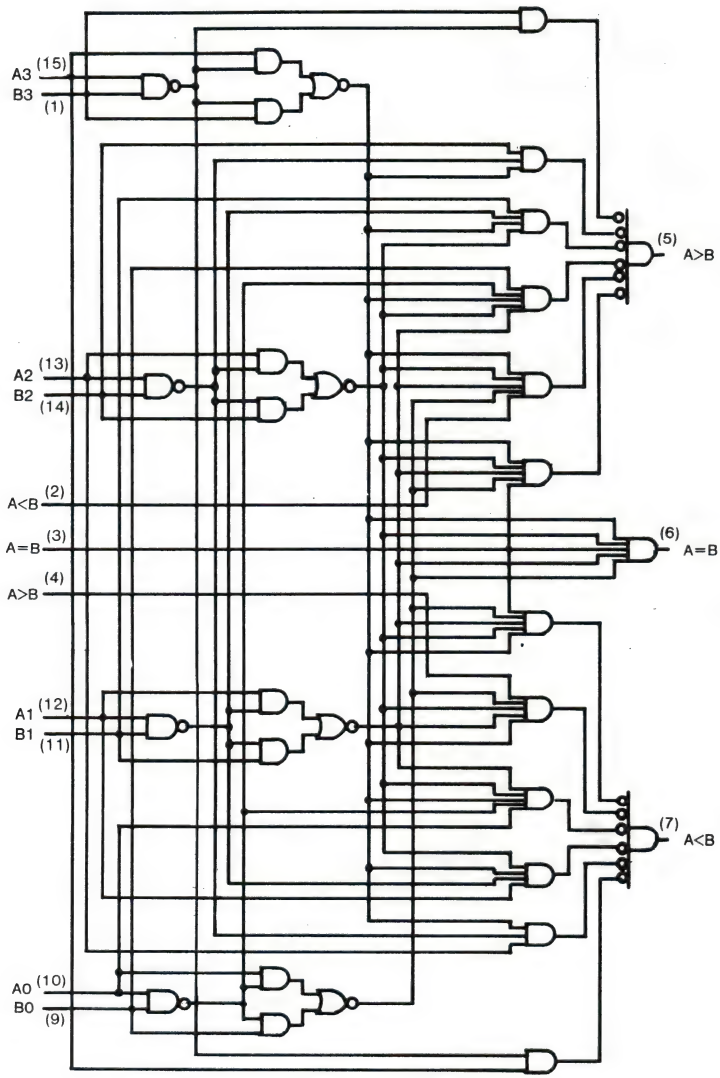
Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

H=High Level, L=Low Level, X=Don't Care

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Function Block Diagram



Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54, 74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	A<B, A>B				0.1	mA
			others				0.3	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	A<B, A>B				20	μA
			others				60	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	A<B, A>B				−0.4	mA
			others				−1.2	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				10	20	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with all inputs at 4.5V, and all outputs open, A=B grounded.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A<B, A>B	1	$C_L=15pF$, $R_L=2k\Omega$,		14		ns
			2			19		
			3			24	36	
		A=B	4			27	45	
t_{PHL}	Any A or B data input	A<B, A>B	1			11		ns
			2			15		
			3			20	30	
		A=B	4			23	45	
t_{PLH}	A<B or A=B	A>B	1			14	22	ns
t_{PHL}	A<B or A=B	A>B	1			11	17	ns
t_{PLH}	A=B	A=B	2			13	20	ns
t_{PHL}	A=B	A=B	2			13	26	ns
t_{PLH}	A>B or A=B	A<B	1			14	22	ns
t_{PHL}	A>B or A=B	A<B	1			11	17	ns

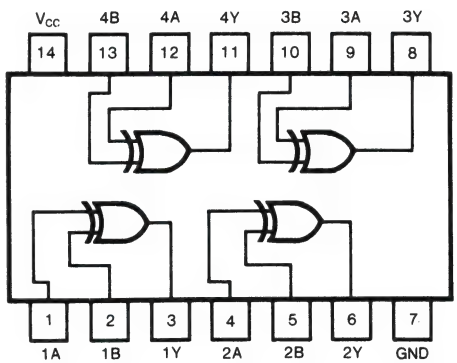
GD54/74LS86

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

Description

This device contains four independent 2-input Exclusive-OR gates. It performs the Boolean functions $Y=A \oplus B=\overline{A}B+A\overline{B}$ in positive logic.

Pin Configuration

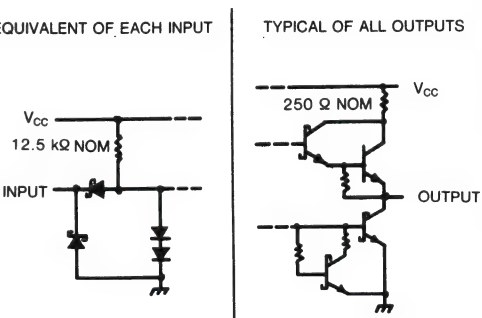


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each gate)

INPUT		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Schematics of Inputs and Outputs



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage				54			0.7	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage		V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
			I_{OH}=Max, V_{IH}=Min		74	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
				I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=7V					0.2	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V					40	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.4V					−0.8	mA
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max				6.1	10	mA
I_{CCL}		Total with outputs low	V_{CC}=Max				9	15	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

Switching Characteristics, V_{CC}=5V, T_A=25°C

PARAMETER*	FROM (INPUT)	TEST CONDITION#		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L=15 pF, R_L=2KΩ		12	23	ns
t_{PHL}					10	17	
t_{PLH}	A or B	Other input high			20	30	ns
t_{PHL}					13	22	

* t_{PLH}=propagation delay time, low-to-high-level output.
* t_{PHL}=propagation delay time, high-to-low-level output.
#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS90
DECADE COUNTERS

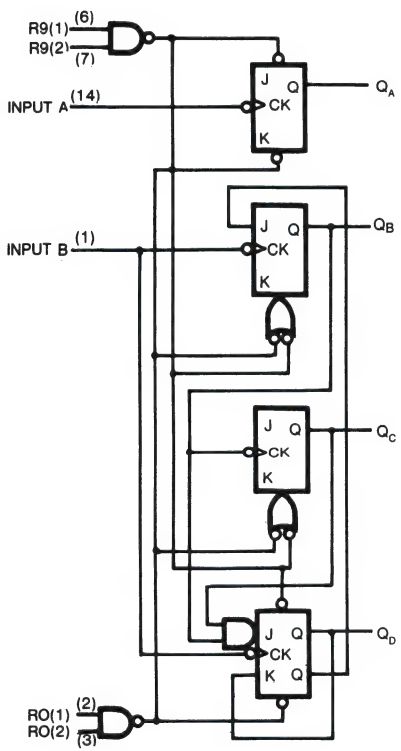
Description

Each of these monolithic counters contains four masterslave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the LS90.

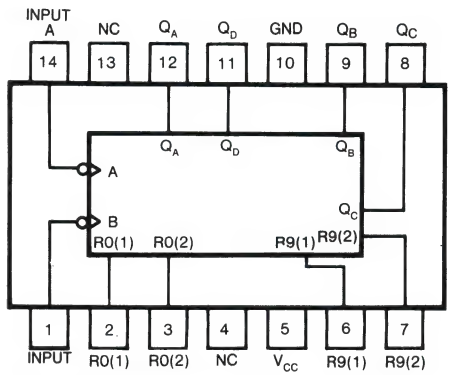
All of these counters have a gated zero reset and the LS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Function Block Diagran



Pin Configuration



NC: No meternal connection

Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

RESET/COUNT TRUTH TABLE

Reset Inputs				Output			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

BCD COUNT SEQUENCE
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	H
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Note A : Output Q_A is connected to input B for BCD count.
B : Output Q_D is connected to input A for bi-quinary.

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54, 74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{count}	Count Frequency	A to Q_A		0		32	MHz
		B to Q_B		0		16	
t_w	Pulse width	A input		15			ns
		B input		30			
		Reset input		15			
t_{REL}	Reset Release Time			25			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage (Note 4)	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	Reset				0.1	mA
		V_{CC}=Max, V_I=5.5V	A				0.2	
			B				0.4	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	Reset				20	μA
			A				40	
			B				80	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	Reset				−0.4	mA
			A				−2.4	
			B				−3.2	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				9	15	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.
Note 4: Q_A outputs are tested at I_{OL}=Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM(INPUT)	TO(OUTPUT)	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}	A	Q_A	$C_L=15pF$ $R_L=2k\Omega$	32	42		MHz
	B	Q_B		16			
t_{PLH}	A	Q_A			10	16	ns
t_{PHL}					12	18	
t_{PLH}	A	Q_D			32	48	ns
t_{PHL}					34	50	
t_{PLH}	B	Q_B			10	16	ns
t_{PHL}					14	21	
t_{PLH}	B	Q_C			21	32	ns
t_{PHL}					23	35	
t_{PLH}	B	Q_D			21	32	ns
t_{PHL}					23	35	
t_{PHL}	Set-to-0	Any			26	40	ns
t_{PLH}	Set-to-9	Q_A,Q_D			20	30	ns
t_{PHL}		Q_B,Q_C			26	40	

* f_{max}=maximum count frequency
* t_{PLH}=propagation delay time, low-to-high-level output.
* t_{PHL}=propagation delay time, high-to-low-level output.

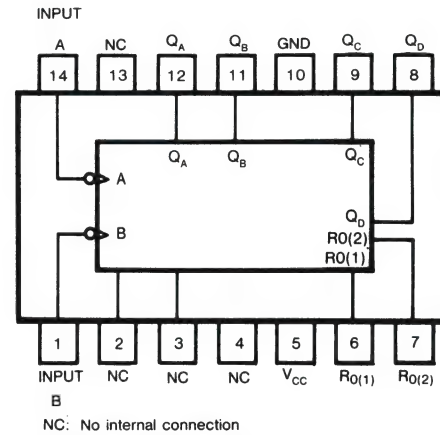
GD54/74LS92

DIVIDE-BY-TWELVE COUNTER

Features

- Direct reset input provided
- Usable independently as binary and divide-by-six counter

Pin Configuration



NC: No internal connection

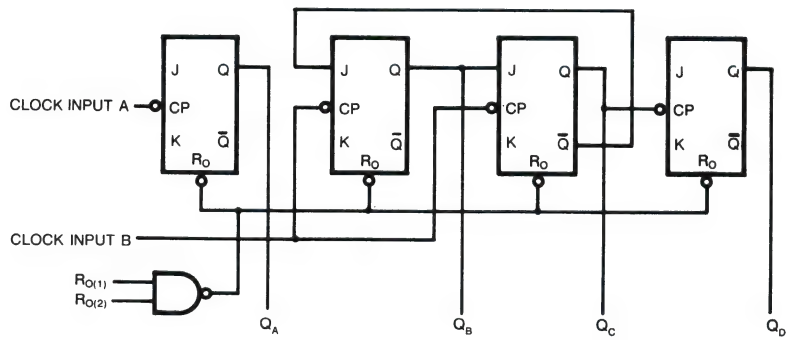
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

This device is composed of independent binary and divide-by-6 counters. Clock input A and output Q_A are employed for use as a binary counter while clock input B and Q_B, Q_C and Q_D are employed for use as a divide-by-6 counter. When employed as a divide-by-12 counter, Q_A and B are connected and by making A the input, the output appears in outputs Q_A, Q_B, Q_C and Q_D in accordance with the function table. The code appearing in the output is not pure binary code. Counting is performed when A and B are changed from high to low.

The binary and divide-by-6 counters can be reset simultaneously by setting direct reset inputs $R_{0(1)}$ and $R_{0(2)}$ high. For use as a counter, either $R_{0(1)}$ or $R_{0(2)}$ or both set low.

Function Block Diagranm and Logic



Reset/Count Function Table

RESET INPUTS		OUTPUT			
Ro(1)	Ro(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

COUNT SEQUENCE
(See Note 1)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

*Note 1: Output Q_A is connected to input B.

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage
  R inputs 7V
  A and B inputs 5.5V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54, 74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{count}	Count frequency	A input		0		32	MHz
		B input		0		16	
t_w	Pulse width	A input		15			ns
		B input		30			
		Reset input		15			
t_{SU}	Reset inactive-state setup time			25			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage (Note 4)	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	Reset				0.1	mA
		V_{CC}=Max, V_I=5.5V	A				0.2	
			B				0.4	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	Reset				20	μA
			A				40	
			B				80	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	A				−0.4	mA
			B				−2.4	
			Reset				−3.2	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max				9	15	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.
Note 4: Q_A outputs are tested at I_{OL}=Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

Switching Characteristics, V_{CC}=5V, T_A=25°C

PARAMETER*	FROM(INPUT)	TO(OUTPUT)	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}	A	Q_A	C_L=15pF, R_L=2kΩ	32	42		MHz
	B	Q_B		16			
t_{PLH}	A	Q_A			10	16	ns
t_{PHL}					12	18	
t_{PLH}	A	Q_D			32	48	ns
t_{PHL}					34	50	
t_{PLH}	B	Q_B			10	16	ns
t_{PLH}					14	21	
t_{PLH}	B	Q_C			10	16	ns
t_{PHL}					14	21	
t_{PLH}	B	Q_D			21	32	ns
t_{PHL}					23	35	
t_{PHL}	Set-to-0	Any			26	40	ns

* f_{max}=maximum count frequency
* t_{PLH}=propagation delay time, low-to-high-level output.
* t_{PHL}=propagation delay time, high-to-low-level output.

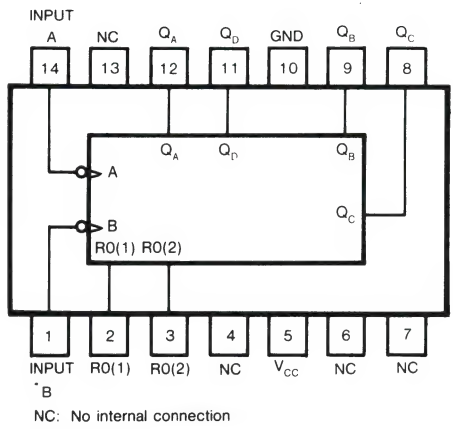
GD54/74LS93

4-BIT BINARY COUNTER DIVIDE-BY-TWO AND DIVIDE-BY-EIGHT

Description

This is an asynchronous 4-bit binary (hexadecimal) counter function with direct reset inputs.
This device is composed of independent binary and octal counters. Clock input A and output Q_A are employed for use as a binary counter while clock input B and Q_B, Q_C and Q_D are employed for use as an octal counter. When employed as a hexadecimal counter, the pure binary code output appears in the Q_A, Q_B, Q_C, and Q_D outputs by connecting Q_A and B, and making A the input. Counting is performed when A and B change from high to low.
The binary and octal counters can be reset simultaneously by setting direct reset inputs $R_{O(1)}$ or $R_{O(2)}$ high. For use as a counter, either $R_{O(1)}$ or $R_{O(2)}$, or both, is set low.

Pin Configuration



NC: No internal connection

Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Count Sequence

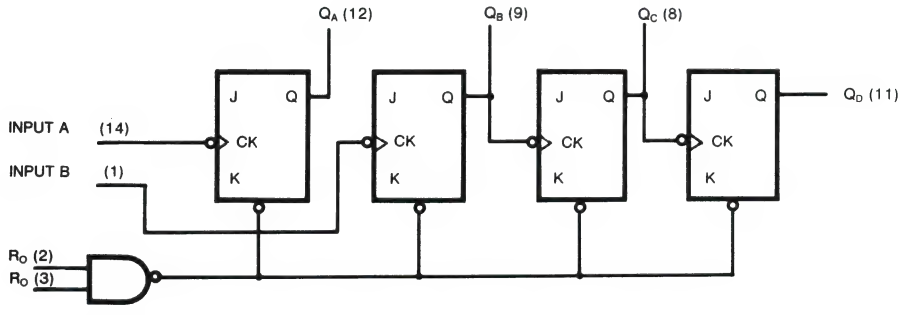
Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

* Output Q_A is connected to input B.

Reset/Count Function Table

Reset Inputs		Output			
RO(1)	RO(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage: R inputs 7V
  A and B inputs 5.5V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	V
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
f_{count}	Count frequency	A input	0		32	MHz
		B input	0		16	
t_W	Pulse width	A input	15			ns
		B input	30			
		Reset input	15			
t_{SU}	Reset inactive-state setup time		25			ns
T_A	Operating free-air temperature		0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage				54			0.7	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage		V_{CC}=Min	V_{IL}=Max	54	2.5	3.4		V
			I_{OH}=Max	V_{IH}=Min	74	2.7	3.4		
V_{OL}	Low-level output voltage (Note 4)		V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
				I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	Any reset	V_{CC}=Max, V_I=7V					0.1	mA
		A or B input	V_{CC}=Max, V_I=5.5V					0.2	
I_{IH}	High-level input current	Any reset	V_{CC}=Max, V_I=2.7V					20	μA
		A or B input						80	
I_{IL}	Low-level input current	Any reset	V_{CC}=Max, V_I=0.4V					−0.4	mA
		A input						−2.4	
		B input						−1.6	
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current		V_{CC}=Max (Note 3)				9	15	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
Note 3: I_{CC} is measured with all outputs open, RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.
Note 4: Q_A outputs are tested at I_{OL}=max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}	A	Q_A	$C_L=15pF$, $R_L=2k\Omega$	32	42		MHz
	B	Q_B		16			
t_{PLH}	A	Q_A			10	16	ns
t_{PHL}					12	18	
t_{PLH}	A	Q_D			46	70	ns
t_{PHL}					46	70	
t_{PLH}	B	Q_B			10	16	ns
t_{PHL}					14	21	
t_{PLH}	B	Q_C			21	32	ns
t_{PHL}					23	35	
t_{PLH}	B	Q_D			34	51	ns
t_{PHL}					34	51	
t_{PHL}	Set-to-0	Any			26	40	ns

* f_{max}=maximum count frequency
* t_{PLH}=propagation delay time, low-to-high-level output.
* t_{PHL}=propagation delay time, high-to-low-level output.

GD54/74LS95B

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

Feature

- Synchronous, expandable shift right
- Synchronous shift left capability
- Synchronous parallel load
- Separate shift and load clock inputs
- Input clamp diodes limit high speed termination effects

Description

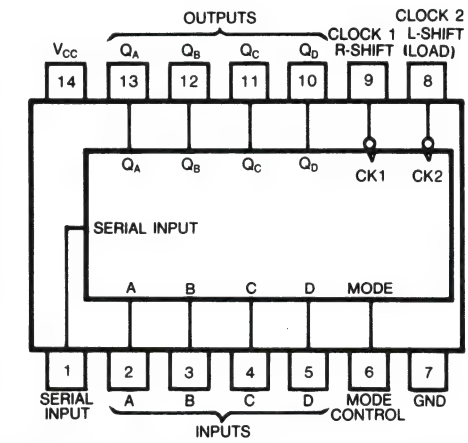
These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

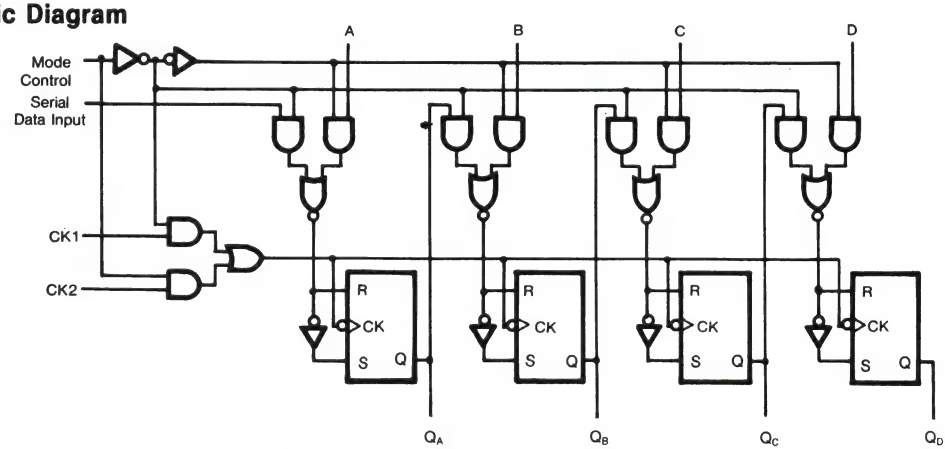
Shift right is accomplished on the high-to-low-transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Logic Diagram



Function Table

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS 2 (L)	CLOCKS 1 (R)	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B↑	Q_C↑	Q_D↑	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

↑Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.
H=high level (steady state), L=low level (steady state), X=irrelevant (any input, including transitions)
↓=transition from high to low level, ↑=transition from low to high level.
a, b, c, d=the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}=the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}= the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54, 74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
f_{clock}	Clock frequency		0		25	MHz
t_w	Width of clock or clear input pulse		20			ns
t_{SU}	Data set up time		20			ns
t_h	Data hold time	54	20			ns
		74	10			
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				13	21	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
Note 3: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded, mode control at 4.5V, and a momentary 3V, then ground, applied to both clock inputs.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L=15pF, R_L=2kΩ	25	36		MHz
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input			18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input			21	32	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS107A

DUAL NEGATIVE-EDGE-TRIGGERED MASTER-SLAVE J-K FLIP-FLOPS WITH CLEAR, AND COMPLEMENTARY OUTPUTS

Features

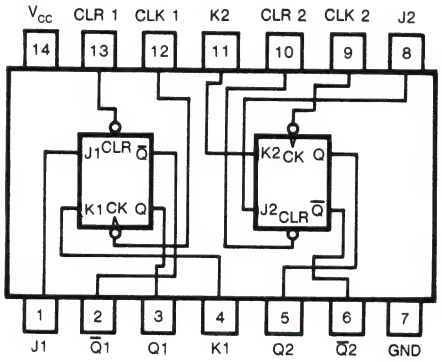
- Negative edge-triggering
- Independent input/output terminals for each flip-flop.
- Direct reset input
- Q and $\overline{Q}$ outputs

Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K inputs must be stable one setup time prior to the High-to-Low clock transition for predictable operation. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J and K inputs may change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the logic levels of the other inputs.

↓=Negative going edge of pulse
Q_o=The output logic level before the indicated input conditions were established.
Toggle=Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Pin Configuration

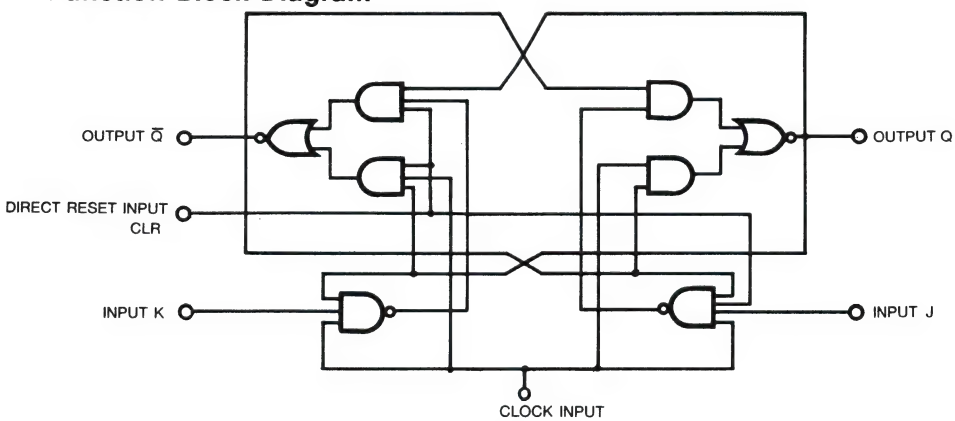


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_o	$\overline{Q}_o$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_o	$\overline{Q}_o$

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54, 74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{clock}	Clock frequency			0		30	MHz
t_w	Pulse Width/enable pulse	Clock High		20			ns
		Clear Low		25			
t_{su}	Data setup time			20↓			ns
t_h	Data hold time			0↓			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	J.K				0.1	mA
			Clear				0.3	
			Clock				0.4	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	J.K				20	μA
			Clear				60	
			Clock				80	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	J,K				−0.4	mA
			Clear				−0.8	
			Clock				−0.8	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				4	6	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed V_o=2.25V and 2.125V for 54 and 74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatc test equipment.
Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

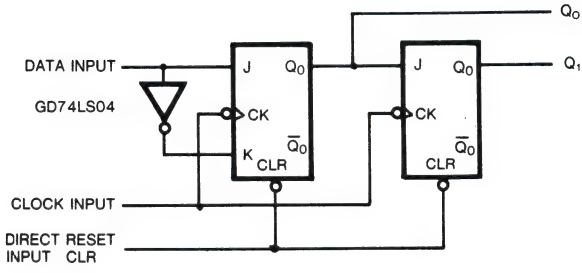
Switching Characteristics, V_{CC}=5V, T_A=25°C

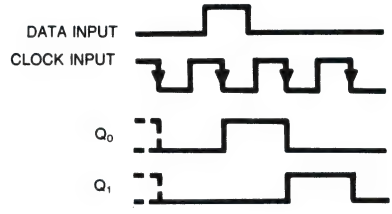
PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}			C_L=15pF, R_L=2kΩ	30	45		MHz
t_{PLH}	Clear	$\overline{Q}$			15	20	ns
t_{PHL}		Q			15	20	
t_{PLH}	Clock	Q or $\overline{Q}$			15	20	ns
t_{PHL}					15	20	

* f_{max}=maximum clock frequency; tested with all outputs loaded.
t_{PLH}=propagation delay time, low-to-high-level output.
t_{PHL}=propagation delay time, high-to-low-level output.
#For load circuit and voltage waveforms, see page 3-11.

Application Example

2BIT SHIFT REGISTER





GD54/74LS109A

DUAL POSITIVE-EDGE-TRIGGERED J-$\overline{K}$ FLIP-FLOPS

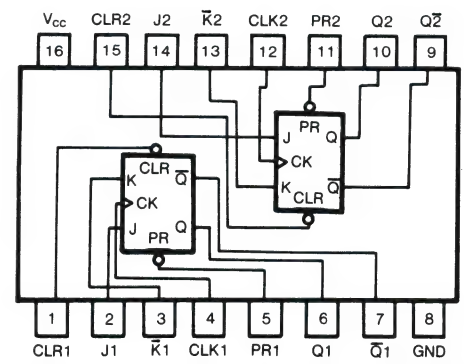
Feature

- Positive Edge-Triggering
- Direct Set and reset inputs
- J and $\overline{K}$ inputs
- Q and $\overline{Q}$ outputs

Description

This device contains two independent positive-edge-triggered J-$\overline{K}$ flip-flops with complementary outputs. The J and $\overline{K}$ data is accepted by the flip-flop on the rising edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the J and $\overline{K}$ inputs may be changed while the clock is high or low as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Pin Configuration



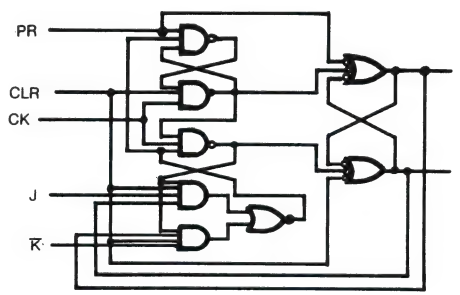
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_o	$\overline{Q}_o$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_o	$\overline{Q}_o$

X = Either Low or High Logic Level
↑ = Rising Edge of Pulse
* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) state.
Q_o = The output logic level of Q before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each active transition of the clock pulse.

Functional Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54,74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{clock}	Clock frequency			0		25	MHz
t_w	Pulse Width	Clock High		18			ns
		Preset Low		15			
		Clear Low		15			
t_{SU}	Setup Time	Data High		30↑			ns
		Data Low		20↑			
t_H	Hold Time			0↑			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
		I_{OH}=Max, V_{IH}=Min		74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	J,$\overline{K}$				0.1	mA
			Clock				0.1	
			Preset				0.2	
			Clear				0.2	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	J,$\overline{K}$				20	μA
			Clock				20	
			Preset				40	
			Clear				40	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	J,$\overline{K}$				−0.4	mA
			Clock				−0.4	
			Present				−0.8	
			Clear				−0.8	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				4	8	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O=2.25V and 2. 125V for 54 and 74 series, respectively, with the minimum and and maximum limits reduced by one half from their stated values. This is very useful when using automastic test equipment.
Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}			$C_L=15pF$, $R_L=2k\Omega$	25	33		MHz
t_{PLH}	Clock	Q or $\overline{Q}$			17	25	ns
t_{PHL}					22	30	ns
t_{PLH}	Clear	$\overline{Q}$			17	25	ns
t_{PHL}		Q			22	30	
t_{PLH}	Preset	Q			16	25	ns
t_{PHL}		$\overline{Q}$			22	30	

* f_{max} = maximum clock frequency.
t_{PLH} = propagation delay time, low-to-level output.
t_{PLH} = propagation delay time, high-to-low-level output.

GD54/74LS112

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH SET AND RESET

Features

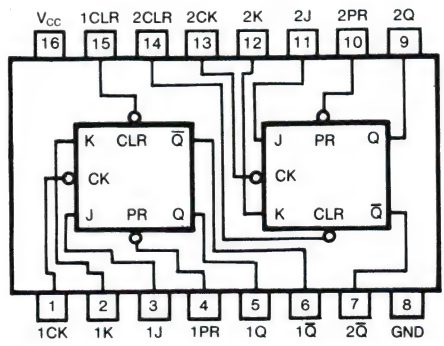
- Negative edge-triggering
- Diode clamped inputs
- Independent input/output terminals for each flip-flop.
- Direct set and reset inputs
- Q and $\overline{Q}$ outputs

Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs can be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

↓=Negative Going Edge of Pulse
•=This configuration is nonstable: that is, it will not persist when preset and/or clear inputs return to their inactive (high) level.
Q_O=The output logic level before the indicated input conditions were established.
Toggle=Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Pin Configuration

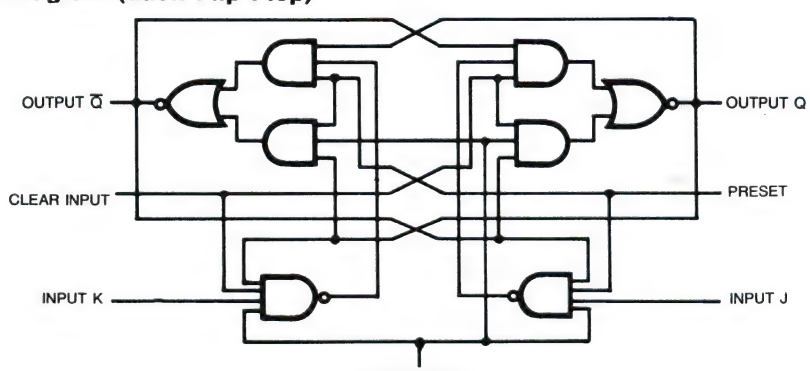


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H•	H•
H	H	↓	L	L	Q_O	$\overline{Q}_O$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_O	$\overline{Q}_O$

Block Diagram (Each Flip Flop)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
t_w	Pulse width	clock high	20		ns
		clock low	25		
		clear or preset low	25		
f_{clock}	Clock frequency		0	30	MHz
t_{su}	Set up time		20↓*		ns
t_h	Input hold time		0↓*		ns
T_A	Operating free-air temperature		0	70	°C

* For falling edge.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max,	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	J,K				0.1	mA
			Clear				0.3	
			Preset				0.3	
			Clock				0.4	
I_{IH}	High-level Input current	V_{CC}=Max, V_I=2.7	J,K				20	μA
			Clear				60	
			Preset				60	
			Clock				80	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	J,K				−0.4	mA
			Clear				−0.8	
			Preset				−0.8	
			Clock				−0.8	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				4	6	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from outputs where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O=2.25V and 2.125V for, 54 and 74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, ICC is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}			C_L=15 pF, R_L=2KΩ	30	45		MHz
t_{PLH}	Clear, preset Clock	Q or $\overline{Q}$			15	20	ns
t_{PHL}					15	20	

*f_{max}=maximum clock frequency
*t_{PLH}=propagation delay time, low-to-high-level output.
*t_{PHL}=propagation delayt ime, high-to-low-level output.

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS123

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

Feature

- D-C Triggered from active-high or active-low gated logic inputs
- Retriggerable for very long output pulses, up to 100% duty cycle
- Overriding clear terminates output pulse
- Compensated for V_{CC} and temperature variations

Description

This D-C triggered multivibrator features output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values.

The LS123 is provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

Output Pulse Width, t_w

The output pulse width tw is set by Rext and Cext

A. When Cext is greater than 1000 pF.
   tw= 0.45·Rext·Cext (ns), Rext: kΩ, Cext; pF.
B. When Cext is equal to or less than 1000 pF, See Figure 1.

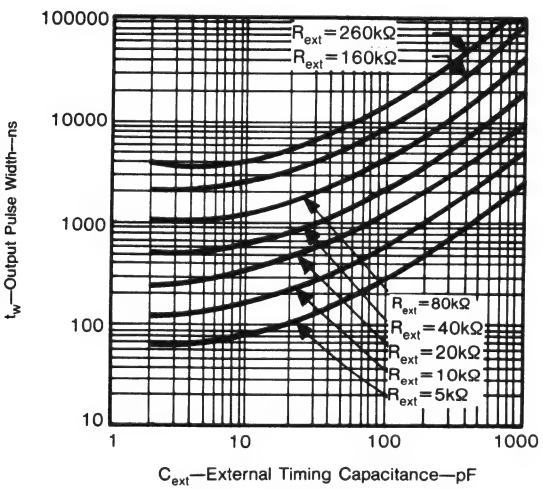
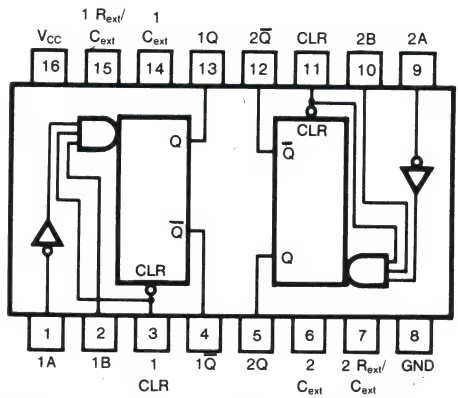


Figure 1. Typical Output Pulse Width VS External Timing Cpacitiance

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

INPUT			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

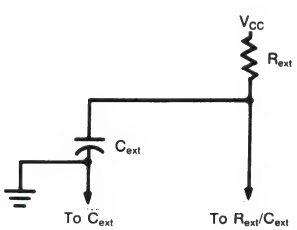


Figure 2. Connection of C_{ext} and R_{ext}

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
t_w	Pulse width		40			ns
R_{ext}	External timing resistance		5		260	KΩ
C_{ext}	External capacitance			No restriction		
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
		I_{OH}=Max, V_{IH}=Min		74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 3)				12	20	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
Note 3: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	$C_{ext}=0$, $R_{ext}=5k\Omega$, $C_L=15pF$, $R_L=2k\Omega$		23	33	ns
	B				23	44	
t_{PHL}	A	$\overline{Q}$			32	45	ns
	B				34	56	
t_{PHL}	Clear	Q			20	27	ns
t_{PLH}		$\overline{Q}$			28	45	
t_wQ (min)	A or B	Q			116	200	ns
t_wQ	A or B	Q	$C_{ext}=1000pF$, $R_{ext}=10k\Omega$, $C_L=15pF$, $R_L=2k\Omega$	4	4.5	5	μs

* t_{PLH}=propagation delay time, low-to-high-level output.
* t_{PHL}=propagation delay time, high-to-low-level output.
* t_wQ=width of pulse at output Q

#For load circuit and voltage waveforms, see page 3-11.

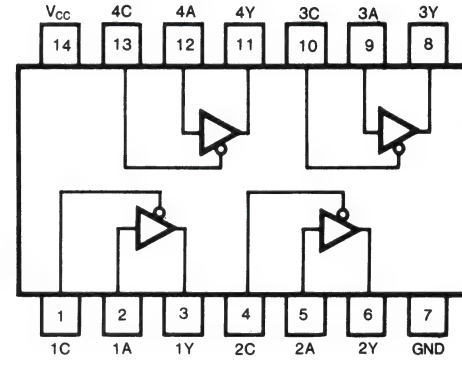
GD54/74LS125A

QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

Description

This device contains 4 buffers with 3-state outputs and is provided with an output control input C which is independent for each buffer.

Pin Configuration



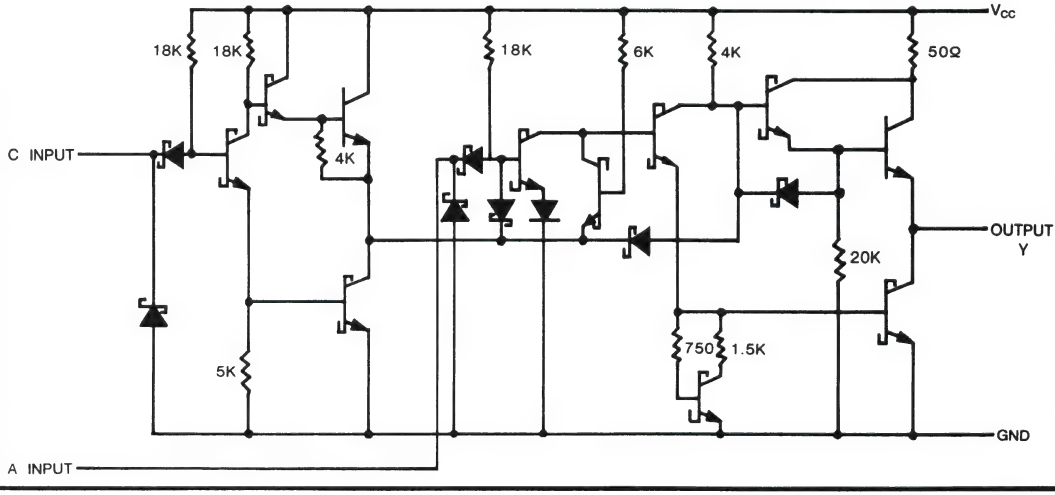
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

INPUTS		OUTPUT
C	A	Y
L	L	L
L	H	H
H	X	Z

X: Irrelevant
Z: High Impedance
Output is off (disabled) when C is high

Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−1	mA
		74			−2.6	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max V_{IH}=Min	I_{OL}=12mA	54,74		0.25	0.4	V
			I_{OL}=24mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−40		−225	mA
I_{OZ}	Off-state (high-impedance state) output current	V_{CC}=Max, V_{IH}=Min V_{IL}=Max,	V_O=2.4V				20	μA
			V_O=0.4V				−20	
I_{CC}	Supply current	V_{CC}=Max Data Input=0V Output control=4.5V				11	20	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=45pF R_L=667Ω		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			7	18	ns
t_{PZH}	Output enable time to high level			12	20	ns
t_{PZL}	Output enable time to low level			15	25	ns
t_{PHZ}	Output disable time from high level	C_L=5pF R_L=667Ω			20	ns
t_{PLZ}	Output disable time from low level				20	ns

#For load circuit and voltage waveforms, see page 3-11.

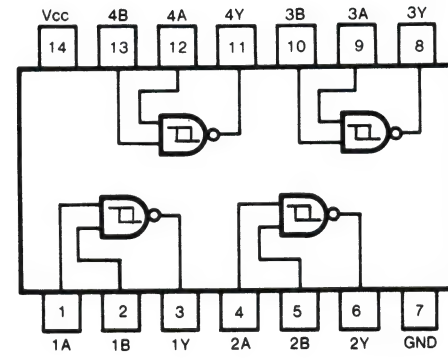
GD54/74LS132

QUAD 2-INPUT NAND GATES WITH SCHMITT TRIGGER INPUTS

Features

- Suitable for waveforms shaping applications
- Wide hysteresis width (0.8V typical) and high noise margin

Pin Configuration



Description

This device contains four independent gates each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.
When inuts A and B are high, output Y is low, and when either or both inputes are low, Y is high.

V_{IN} VERSUS V_{OUT} TRANSFER FUNCTION

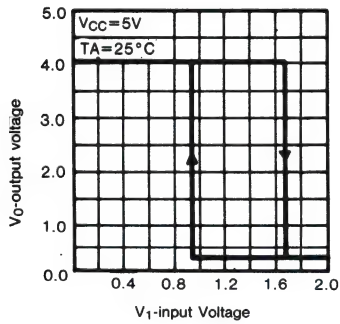


Fig. 1

Function Table

A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

$Y=\overline{AB}$

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	V_{CC}=5V			1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	V_{CC}=5V			0.5	0.8	1	V
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{T+}, V_{T-}	Input Hysteresis (Note 1)	V_{CC}=5V			0.4	0.8		V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max, V_I=V_{T-}Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_I=V_{T+}Max	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC}=5V, V_I=V_{T+}				−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC}=5V, V_I=V_{T-}				−0.18		mA
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max				5.9	11	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max				8.2	14	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	22	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS138

3-TO-8-LINE DECODERS/DEMULTIPLEXERS

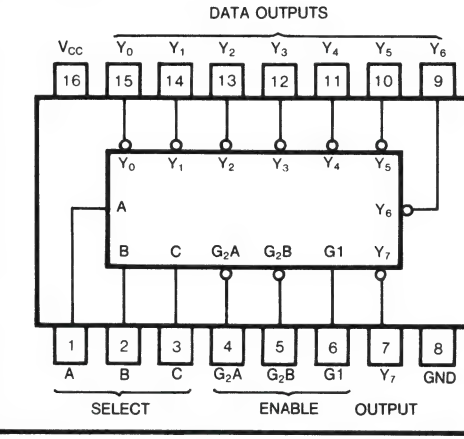
Feature

- Designed Specifically for High Speed Memory Decoders and Data Transmission Systems
- Incorporate 3 Enable Inputs to Simplify Cascading AND/OR Data Reception
- Schottky Clamped for High Performance

Description

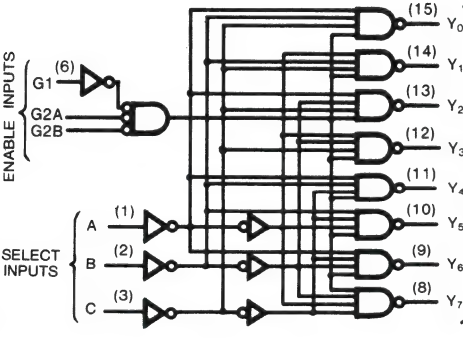
This schottky-clamped TTL MSI circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay time. In high-performance memory systems this decode can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit the delay times of this decoder and the enable time of the memory are usually less than the typical access times of the memory. This means that the effective system delay introduced by the schottky-clampled system decoder is negligible.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Block Diagram and Logic



Function Table

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

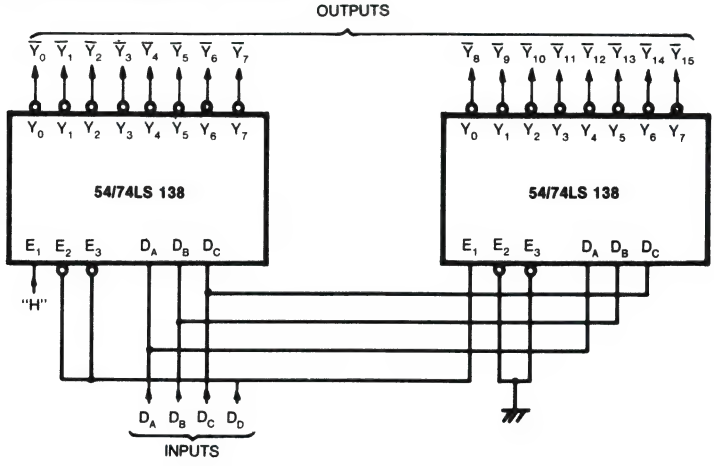
* G2=G2A+G2B

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Application Example

4-LINE TO 16-LINE DECORDER/DEMULTIPLEXER



Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max, Outputs enabled and open				6.3	10	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LEVEL	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Binary Select	Any	2	$C_L=15pF$ $R_L=2k\Omega$		13	20	ns
t_{PHL}						27	41	ns
t_{PLH}			3			18	27	ns
t_{PHl}						26	39	ns
t_{PLH}	Enable	Any	2			12	18	ns
t_{PHL}						21	32	ns
t_{PLH}			3			17	26	ns
t_{PHL}						25	38	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS139

DUAL 2-TO-4-LINE DECODERS/DEMULTIPLEXERS

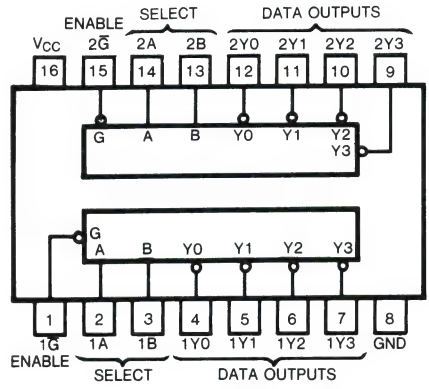
Feature

- Designed Specifically for High Speed Memory Decoders and Data Transmission Systems
- Schottky Clamped for High Performance

Description

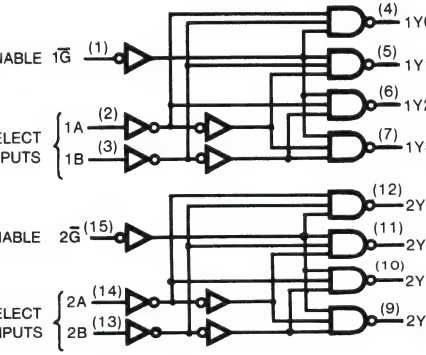
This schottky-clamped TTL MSI circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by schottky-clamped system decoder is neglible.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Block Diagram and Logic



Function Table

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H: High level
L: Low level
X: Irrelevant

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
		I_{OH}=Max, V_{IH}=Min		74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V, Outputs enabled and open				6.8	11	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

Switching Characteristics, V_{CC}=5V, T_A=25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LEVEL	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Binary Select	Any	2	C_L=15pF, R_L=2kΩ		13	20	ns
t_{PHL}						22	33	ns
t_{PLH}			3			18	29	ns
t_{PHL}						25	38	ns
t_{PLH}	Enable	Any	2			16	24	ns
t_{PHL}						21	32	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS145

BCD-TO-DECIMAL DECODER/DRIVER

Features

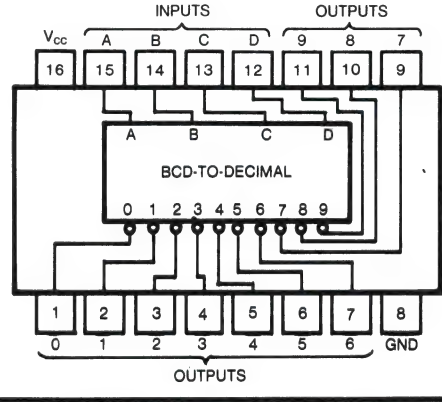
- Full Decoding of Input Logic
- 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions
- Low Power Dissipation of 'LS145...35 mW Typical

Description

These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remains off for all invalid binary input conditions. These decoders feature high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers.

The outputs are open collector types with a breakdown voltage of 15V and an I_{OL} of 80mA (with $V_{OL} \leqq 3V$) This device is therefore suitable for use as an LSTTL/MOS interface, display tube and relay driver.

Pin Configuration



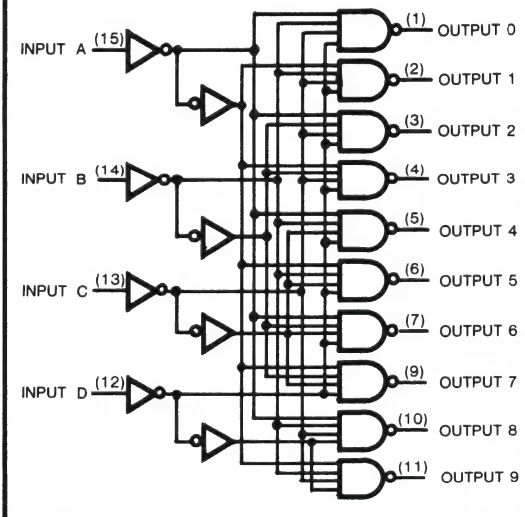
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	H	L	H	L	H	H	H	H	H	H	H	H	H	H
11	H	L	H	H	H	H	H	H	H	H	H	H	H	H
12	H	H	L	L	H	H	H	H	H	H	H	H	H	H
13	H	H	L	H	H	H	H	H	H	H	H	H	H	H
14	H	H	H	L	H	H	H	H	H	H	H	H	H	H
15	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H=high level (off), L=low level (on)

Functional Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
V_O	Off-State output voltage	54,74			15	V
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
$I_{O(Off)}$	Off-state output current	V_{CC}=Min, V_{OH}=Max					250	μA
$V_{O(ON)}$	On-state output voltage	V_{CC}=Min	I_{OL}=12mA	54,74		0.25	0.4	V
		V_{IL}=Max	I_{OL}=24mA	74		0.35	0.5	
		V_{IH}=Min	I_{OL}=80mA	74		2.3	3.0	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{CC}	Supply current	V_{CC}=Max (Note 2)				7	13	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: I_{CC} is measured with all inputs grounded and outputs open.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=45pF, R_L=665Ω		50	ns
t_{PHL}	Propagation delay time, high-to-low-level output			50	ns

#For load circuit and voltage waveforms, see page 3-11.

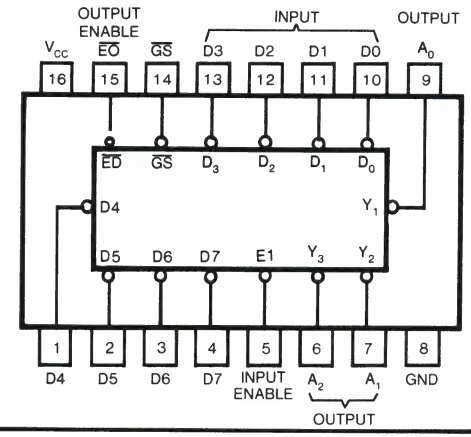
GD54/74LS148

8-TO-3 LINE PRIORITY ENCODER

Features

- Priority Decoding of the Data Inputs
- Code conversions
- Decimal-to-BCD Converter
- Group Serial Output active when any input is low

Pin Configuration



Sufix-Blank: Plastic Dual In Line Package
Sufix J : Ceramic Dual In Line Package

Description

These priority encoder provide on 8 line to 3 line priority encoder function and priority sequence function.

A priority is given to each input the highest level input pin signal is encoded when two or more inputs are simultaneously active.

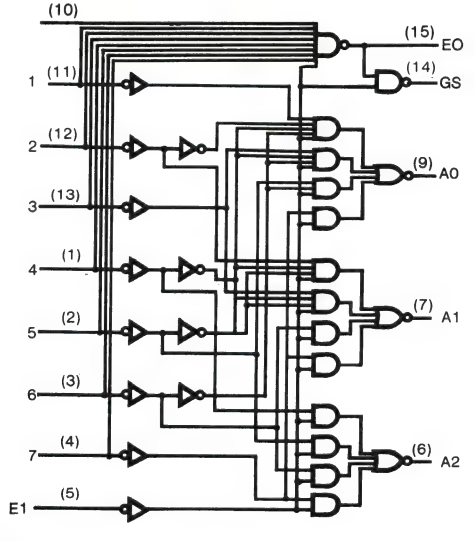
The number of input data can be easily increased by using the enable inupt E output enable $\overline{E0}$ and group serial output $\overline{GS}$.

This device is suitable for use as a key board encoder.

Function Table

INPUTS									OUTPUTS				
E1	D0	D1	D2	D3	D4	D5	D6	D7	A2	A1	A0	GS	E0
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

Functional Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	Typ (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	Input D0~D7				0.2	mA
			All other inputs				0.1	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	Input D0~D7				40	μA
			All other inputs				20	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	Input D0~D7				−0.8	mA
			All other inputs				−0.4	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)	Condition A			12	20	mA
			Condition B			10	17	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
Note 3: Condition A: I_{CC} is measured with input D4 and E1 grounded, other inputs and outputs oepn.
Condition B: I_{CC} is measured with all inputs and outputs open.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	D1~D7	Y1, Y2, Y3	$C_L=15pF$ $R_L=2k\Omega$		14	18	ns
t_{PHL}	(levels of delay 2)				15	25	
t_{PLH}	D1~D7	Y1, Y2, Y3			20	36	ns
t_{PHL}	(level of delay 3)				16	29	
t_{PLH}	D0~D7	E0			7	18	ns
t_{PHL}	(levels of delay 3)				25	40	
t_{PLH}	D0~D7	GS			35	55	ns
t_{PHL}	(levels of delay 2)				9	21	
t_{PLH}	E1	Y1, Y2, Y3			16	25	ns
t_{PHL}	(levels of delay 2)				12	25	
t_{PLH}	E1	GS			12	17	ns
t_{PHL}	(levels of delay 2)				14	36	
t_{PLH}	E1	E0			12	21	ns
t_{PHL}	(levels of delay 2)				23	35	

* t_{PLH} = propagation delay time, low-to-high-level output
* t_{PHL} = propagation delay time, high-to-low-level output

For load circuit and voltage waveforms, see page 3-11.

GD54/74LS151

DATA SELECTOR/MULTIPLEXER

Features

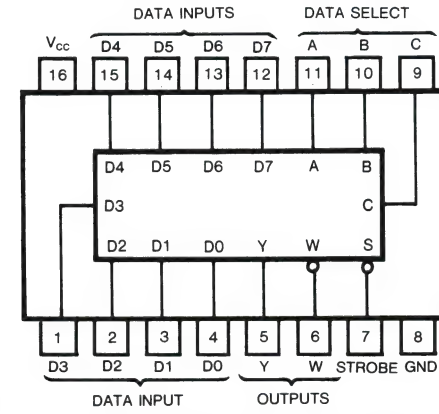
- Select one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use Boolean function generator

Description

This data selector/multiplexer contains full on-chip decoding to select the desired data source. The LS151 selects one-of-eight data sources. The LS151 has a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output low.

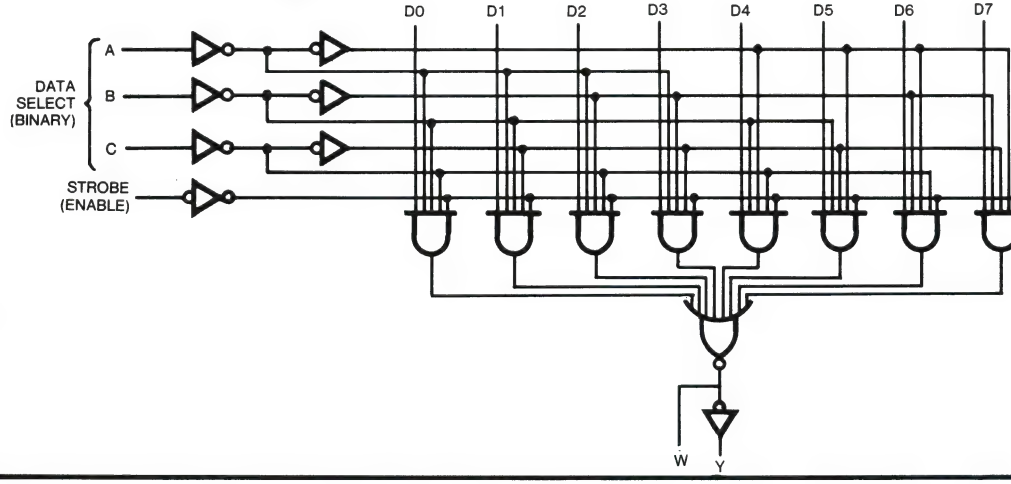
The LS151 features complementary W and Y outputs.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Functional Block Diagram



Function Table

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H=High Level, L=Low Level, Irrelevant
D0,D1...D7=the level of the respective D input

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
		I_{OH}=Max, V_{IH}=Min		74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				6	10	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with all outputs open, strobe and data select inputs at 4.5V, and all other inputs open.

Switching Characteristics, V_{CC}=5V, T_A=25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION #	MIN	TYP	MAX	UNIT
t_{PLH}	A,B or C(4 levels)	Y	C_L=15pF, R_L=2KΩ		27	43	ns
t_{PHL}					18	30	
t_{PLH}	A,B or C(3 levels)	W			14	23	ns
t_{PHL}					20	32	
t_{PLH}	Any D	Y			20	32	ns
t_{PHL}					16	26	
t_{PLH}	Any D	W			13	21	ns
t_{PHL}					12	20	
t_{PLH}	Strobe	Y			26	42	ns
t_{PHL}					20	32	
t_{PLH}	Strobe	W			15	24	ns
t_{PHL}					18	30	

* t_{PLH}= propagation delay time, low-to-high-level output
* t_{PHL}= propagation delay time, high-to-low-level output

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS153

DUAL 4-LINE TO 1 – LINE DATA SELECTORS/MULTIPLEXERS

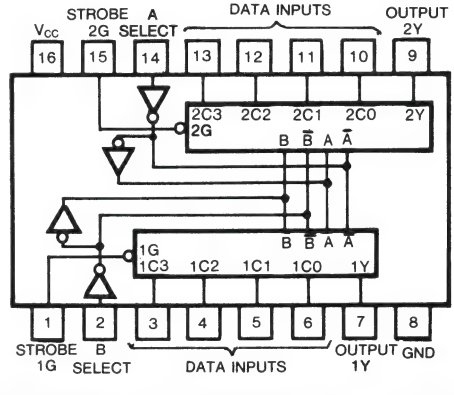
Feature

- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)
- High-Fan-Out, Low-Impedance, Totem Pole Outputs
- Fully Compatible with Most TTL and DTL Circuits

Description

This monolithic data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip binary decoding data selection to the AND/OR invert gates. Separate strobe inputs are provided for each of the two four line sections.

Pin Configuration

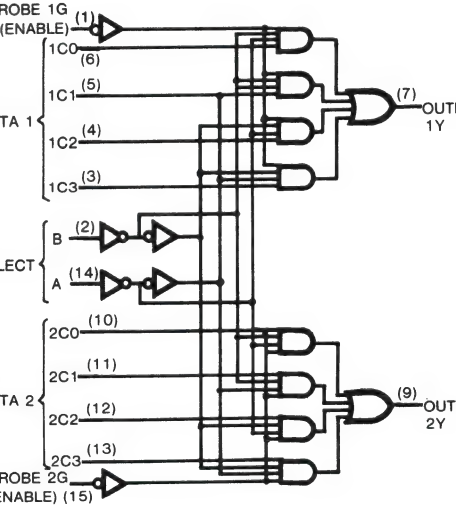


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

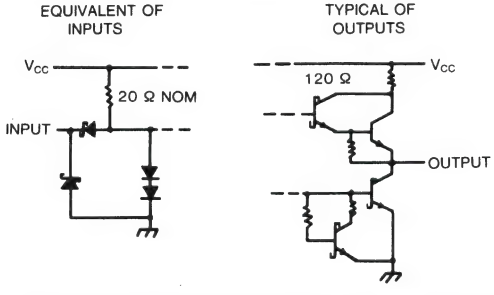
Function Table

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Functional Block Diagram



Schematics of Inputs and Outputs



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
		I_{OH}=Max, V_{IH}=Min		74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCL}	Supply current	V_{CC}=5.25V (Note 3)				7.4	12	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
Note 3: I_{CCL} is measured with the outputs open and all inputs grounded.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L=15 pF, R_L=2kΩ		10	15	ns
t_{PHL}	Data	Y			17	26	ns
t_{PLH}	Select	Y			19	29	ns
t_{PHL}	Select	Y			25	38	ns
t_{PLH}	Strobe	Y			16	24	ns
t_{PHL}	Strobe	Y			21	32	ns

#For load circuit and voltage waveforms, see page 3-11.

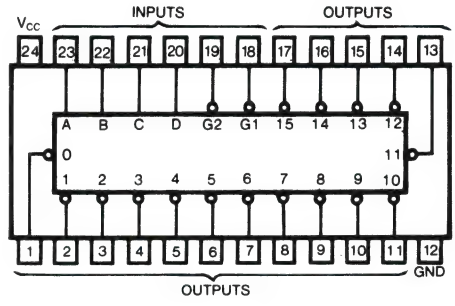
GD54/74LS154

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS

Feature

- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data from One Input Line to Any One of 16 Outputs
- Input Clamping Diodes Simplify System Design
- High Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with Most TTL, DTL and MSI Circuits

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

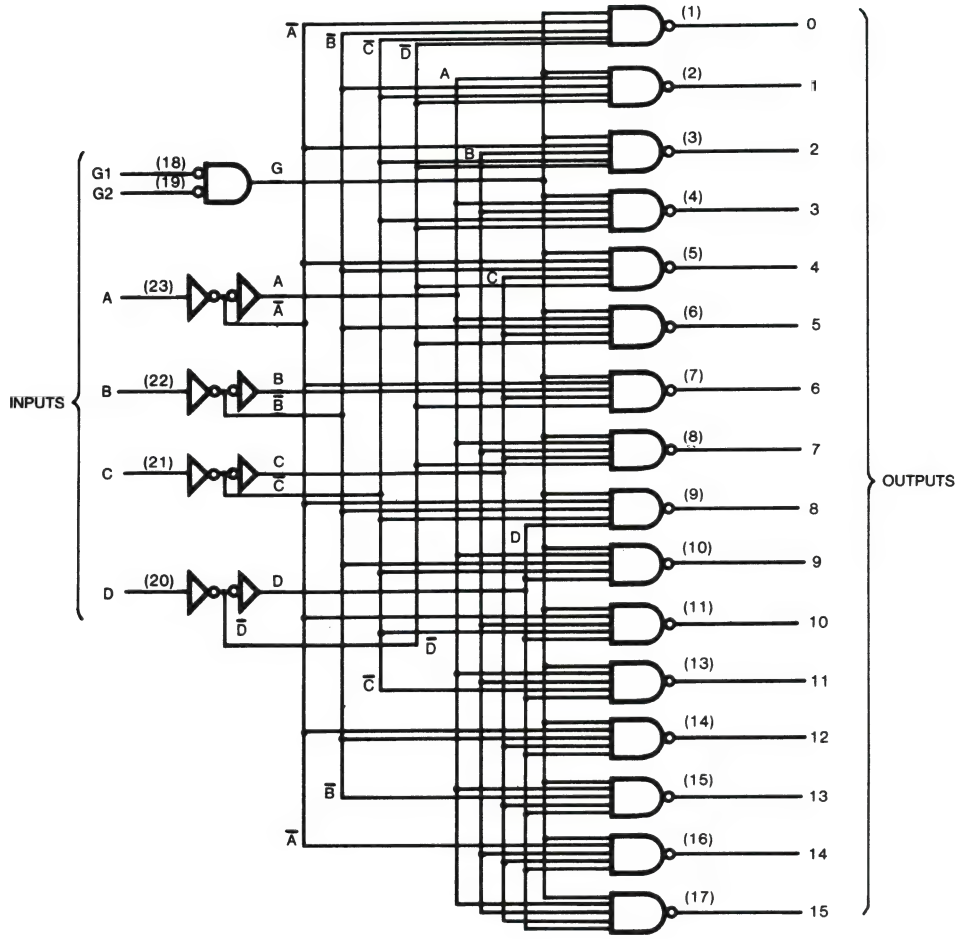
This monolithic 4-line to 16 line decoder utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G_1 and G_2 are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.

Function Table

INPUTS						OUTPUTS													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

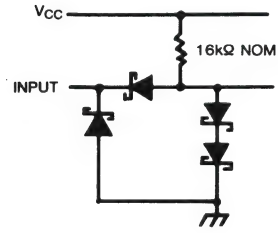
H: High level L: Low level X: Irrelevant

Function Block Diagram

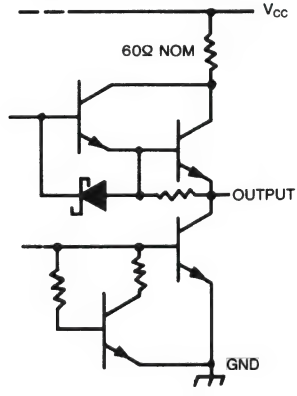


Schematics of Inputs and Outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				9	14	mA

Note 1: All typicals are at V_{CC}=V, T_A=25°C
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with the inputs grounded and all outputs open.

Switching Characteristics V_{CC}=5V, T_A=25°C

SYMBOL	TEST CONDITIONS#		MIN	TYP	MAX	UNIT
t_{PLH}	Data to output	C_L=15pF, R_L=2kΩ		22	36	ns
t_{PHL}	Data to output			22	33	ns
t_{PLH}	Strobe to output			18	30	ns
t_{PHL}	Strobe to output			16	27	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS155

DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

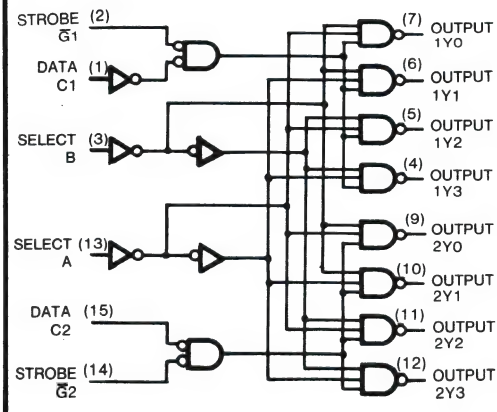
Features

- Applications:
  - Dual 2-to-4-line decoder
  - Dual 1-to-4-line demultiplexer
  - 3-to-8-line decoder
  - 1-to-8-line demultiplexer
- Individual strobes simplify cascading for decoding or demultiplexing larger words
- Input clamping diodes simplify system design

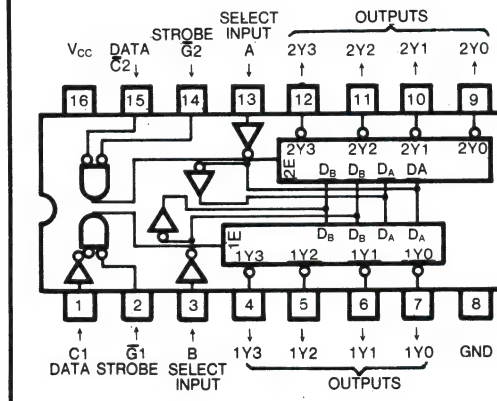
Description

These TTL circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied at $\overline{C2}$ is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demultiplexers, without external gating. Input clamping diodes are provided on these circuits to minimize transmission-line effects and simplify system design.

Functional Block Diagram



Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Tables

2-Line-to-4-Line Decoder or 1-Line-to-4-Line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data				
B	A	$\overline{G1}$	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	L	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	$\overline{G2}$	$\overline{C2}$	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer

Inputs				Outputs							
Select			Strobe Or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C*	B	A	G**	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

C* = inputs C1 and $\overline{C2}$ connected together
G** = inputs $\overline{G1}$ and $\overline{G2}$ connected together
H = high level L = low level X = don't care

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply votage	54	4.5		5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max,	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		54	−20		−100	mA
				74	−20		−100	
I_{CC}	Supply current	V_{CC}=Max (Note 3)				6.1	10	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with all outputs open, A, B, and C1 inputs at 4.5V, and $\overline{C2}$, $\overline{G1}$, and $\overline{G2}$ inputs grounded.

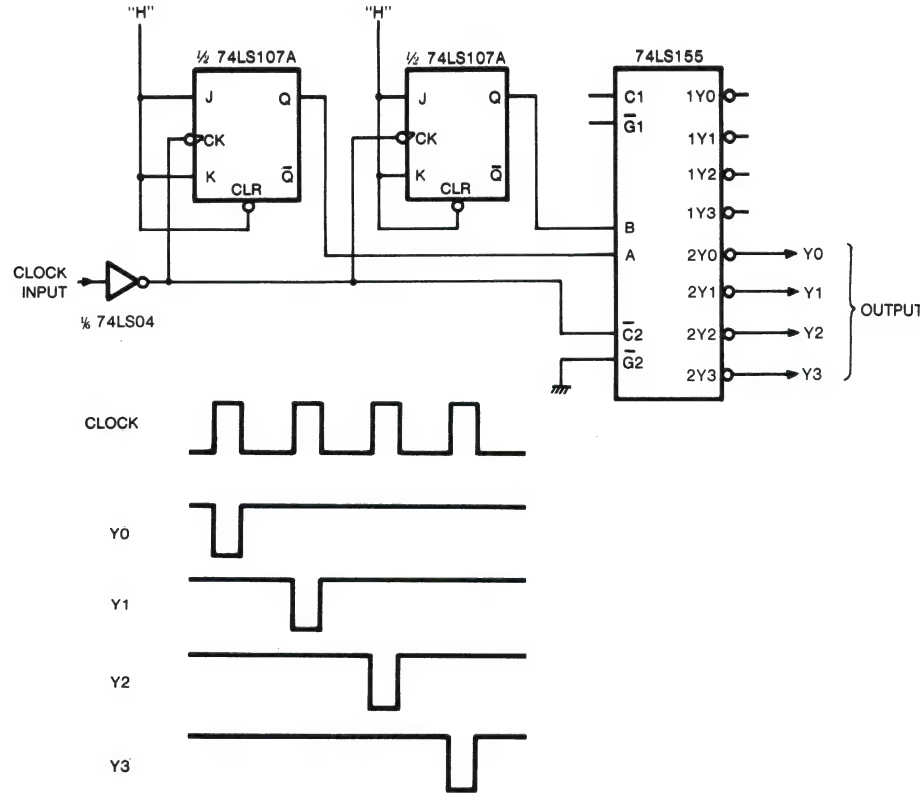
Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	54LS155 74LS155 MIN	TYP	MAX	UNIT
t_{PLH}	A, B, $\overline{C2}$ $\overline{G1}$ or $\overline{G2}$	Y	2	$C_L=15pF$, $R_L=2k\Omega$, See Note 4		10	15	ns
t_{PHL}	A, B, $\overline{C2}$ $\overline{G1}$ or $\overline{G2}$	Y	2			19	30	ns
t_{PLH}	A or B	Y	3			17	26	ns
t_{PHL}	A or B	Y	3			19	30	ns
t_{PLH}	C1	Y	3			18	27	ns
t_{PHL}	C1	Y	3			18	27	ns

t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 3-11.

Application Example

4-PHASE CLOCK PULSE GENERATOR



GD54/74LS157

QUADRUPLE 2-TO-1-LINE DATA SELECTORS/MULTIPLEXERS (NON INVERTED DATA OUTPUTS)

Feature

- Buffered Inputs and Outputs
- Common Strobe/Select input for all 4 circuits.

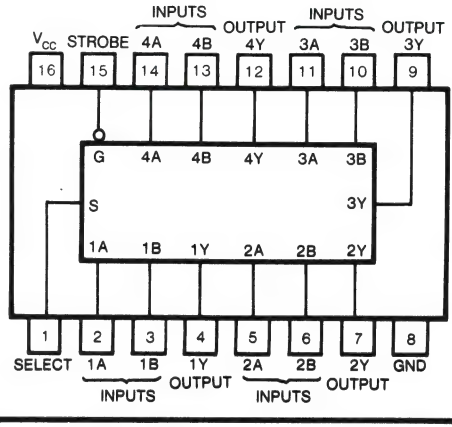
Descriptions

This monolitic data selector/multiplexer contains inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The LS157 has the same functions and pin connections as the LS257 but the latter is provided with 3-state outputs.

Applications

- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables (One Variabes Is Common)
- Source Programmable Counters

Pin Configuration



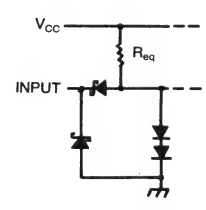
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

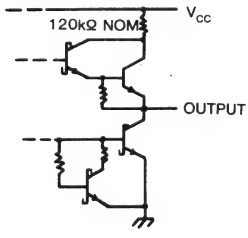
INPUTS				OUTPUT
STROBE	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Schematics of Inputs and Outputs

EQUIVALENT OF EACH INPUT

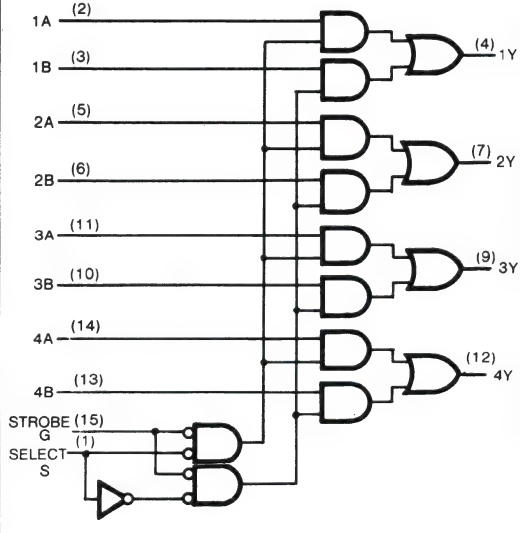


TYPICAL OF ALL OUTPUTS



S or G inputs: R_{eq} = 8.5 kΩ NOM
A or B inputs: R_{eq} = 17 kΩ NOM

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−12mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IH}=Min, V_{IL}=Max, I_{OH}=Max		54	2.5	3.4		μA
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V		S or G input			0.2	mA
				A or B input			0.1	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V		S or G input			40	μA
				A or B input			20	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V		S or G input			−0.8	mA
				A or B input			−0.4	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				9.6	16	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with all outputs open, and 4.5V applied to all inputs.

Switching Characteristics, V_{CC}5V, T_A=25°C

PARAMETER*	FROM (INPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Data	C_L=15pF, R_L=2kΩ		9	14	ns
t_{PHL}				9	14	
t_{PLH}	Strobe			13	20	ns
t_{PHL}				14	21	
t_{PLH}	Select			15	23	ns
t_{PHL}				18	27	

* t_{PLH}=propagation delay time, low-to-high-level output.
* t_{PHL}=propagation delay time, high-to-low-level output.
# For load circuit and voltage waveforms, see page 3-11.

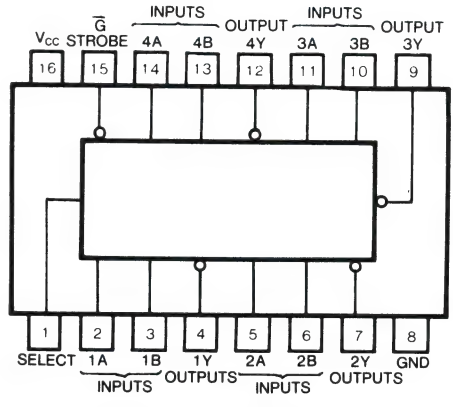
QUADRUPLE 2-TO-1-LINE DATA SELECTORS/MULTIPLEXERS (INVERTED DATA OUTPUTS)

GD54/74LS158

Features

- Buffered Inputs and Outputs
- Converted outputs provided.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

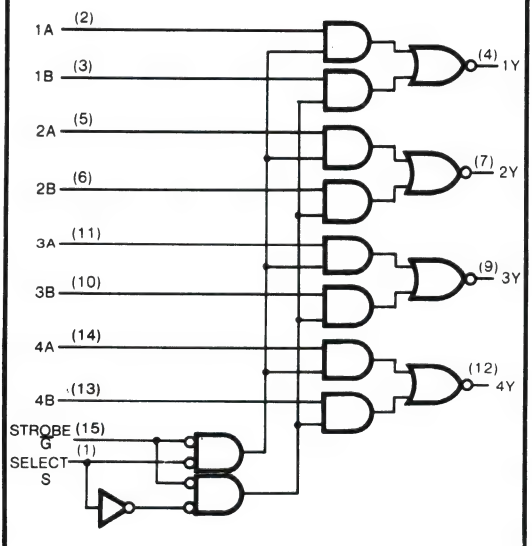
Applications

- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables (One Variables is Common)
- Source Programmable Counters

Description

This monolitic data selector/multiplexer contains inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The LS158 presents inverted data to minimize propagation delay time.

Function Block Diagram



Function Table

INPUTS				OUTPUT
STROBE	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−12mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IH}=Min, V_{IL}=Max, I_{OH}=Max		54	2.5	3.4		μA
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	54		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V		S or G input			0.2	mA
				A or B input			0.1	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V		S or G input			40	μA
				A or B input			20	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V		S or G input			−0.8	mA
				A or B input			−0.4	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				4.8	8	mA
		V_{CC}=Max (Note 4)				6.5	11	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with all outputs open, and all inputs at 4.5V
Note 4: I_{CC} is measured with all A inputs at 4.5V and all other inputs at 0V.

Switching Characteristics, V_{CC}5V, T_A=25°C

PARAMETER*	FROM (INPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Data	C_L=15pF, R_L=2kΩ		7	14	ns
t_{PHL}				10	14	
t_{PLH}	Strobe			11	20	ns
t_{PHL}				18	21	
t_{PLH}	Select			13	23	ns
t_{PHL}				16	27	

* t_{PLH}=propagation delay time, low-to-high-level output.
* t_{PHL}=propagation delay time, high-to-low-level output.
# For load circuit and voltage waveforms, see page 3-11.

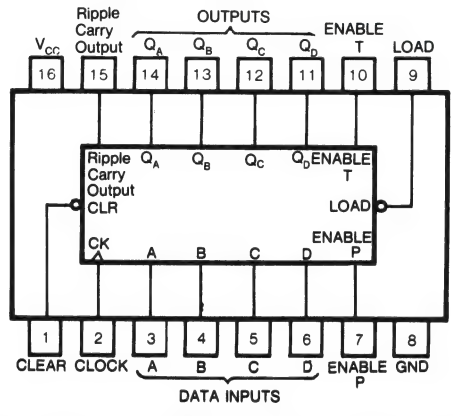
GD54/74LS161A

SYNCHRONOUS 4 BIT COUNTERS; BINARY, DIRECT CLERAR

Feature

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

This synchronous, presettable counter features an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change conicident with each other when so instructed by the count-enable inputs and internal gating.

This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input wave form.

This counter is fully programmable; that is the outputs may be preset to either level. As presetting is synchronous setting up a low level at the load input disables the counter and causes the outputs to agree with the setup dsta after the next clock pulse regardless of the levels of the enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two counter-enable inputs and a riple carry output. Both countenable inputs (ENABLE P and ENABLE T) must be high to count, and ENABLE T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high level portion of the Q_A output. The high-level overflow riple carry pulse can be enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

Function Table (Note 1)

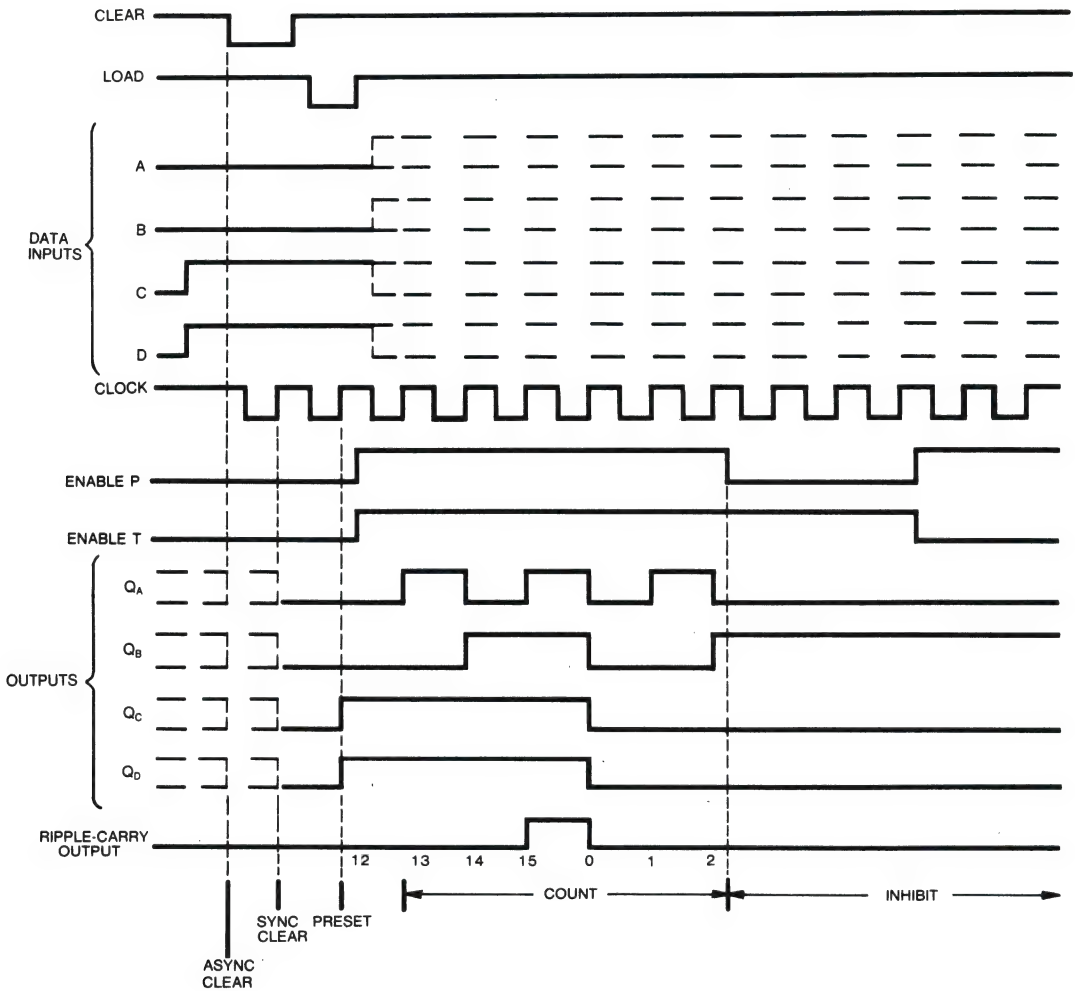
$\overline{CLR}$	$\overline{LOAD}$	E_T	E_P	CK	Q_A	Q_B	Q_C	Q_D	RCO
L	X	X	X	X	L	L	L	L	L
H	L	L	X	↑	D_A	D_B	D_C	D_D	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Inhibit				L
H	H	H	L	X	Inhibit				L*

Note 1: ↑ : Indicates a transition from low to high (positive edge triggering).
* : RCO is normally low but is high when all Q outputs and E_T are high simultaneously, i.e.,
$RCO = Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot E_T$
X : irrelevant

Typical Clear, Preset, Count, and Inhibit Sequences

Illustrated below is the following sequence:

1. Clear outputs to zero (asynchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54,74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{clock}	Clock frequency			0		25	MHz
$tw_{(clock)}$	Width of clock pulse			25			ns
$tw_{(clear)}$	Width of clear pulse			20			ns
t_{SU}	Setup time	Data inputs A,B,C,D.		20			ns
		Enable P or T		20			
		Load		20			
t_h	Hold time at any input			3			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	Data or enable P				0.1	mA
			Load, clock or enable T				0.2	
			Clear				0.1	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	Data or enable P				20	μA
			Load, clock or enable T				40	
			Clear				20	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	Data or enable P				−0.4	mA
			Load, clock or enable T Clear				−0.8	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=Max (Note 3)				18	31	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=Max (Note 4)				18	32	mA

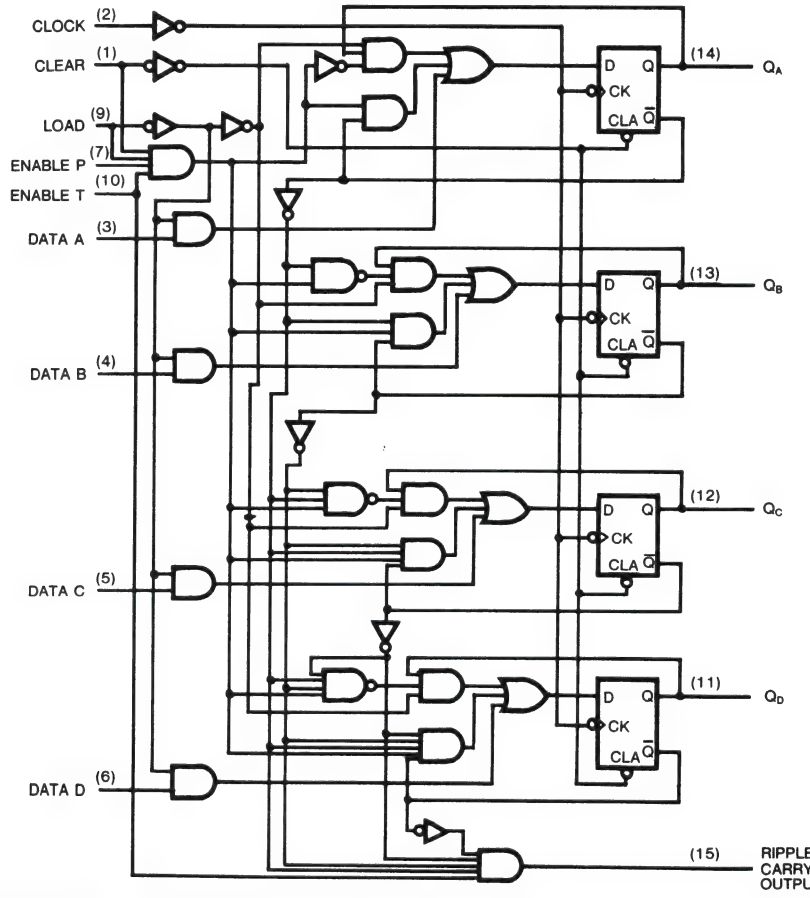
Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.
Note 4: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

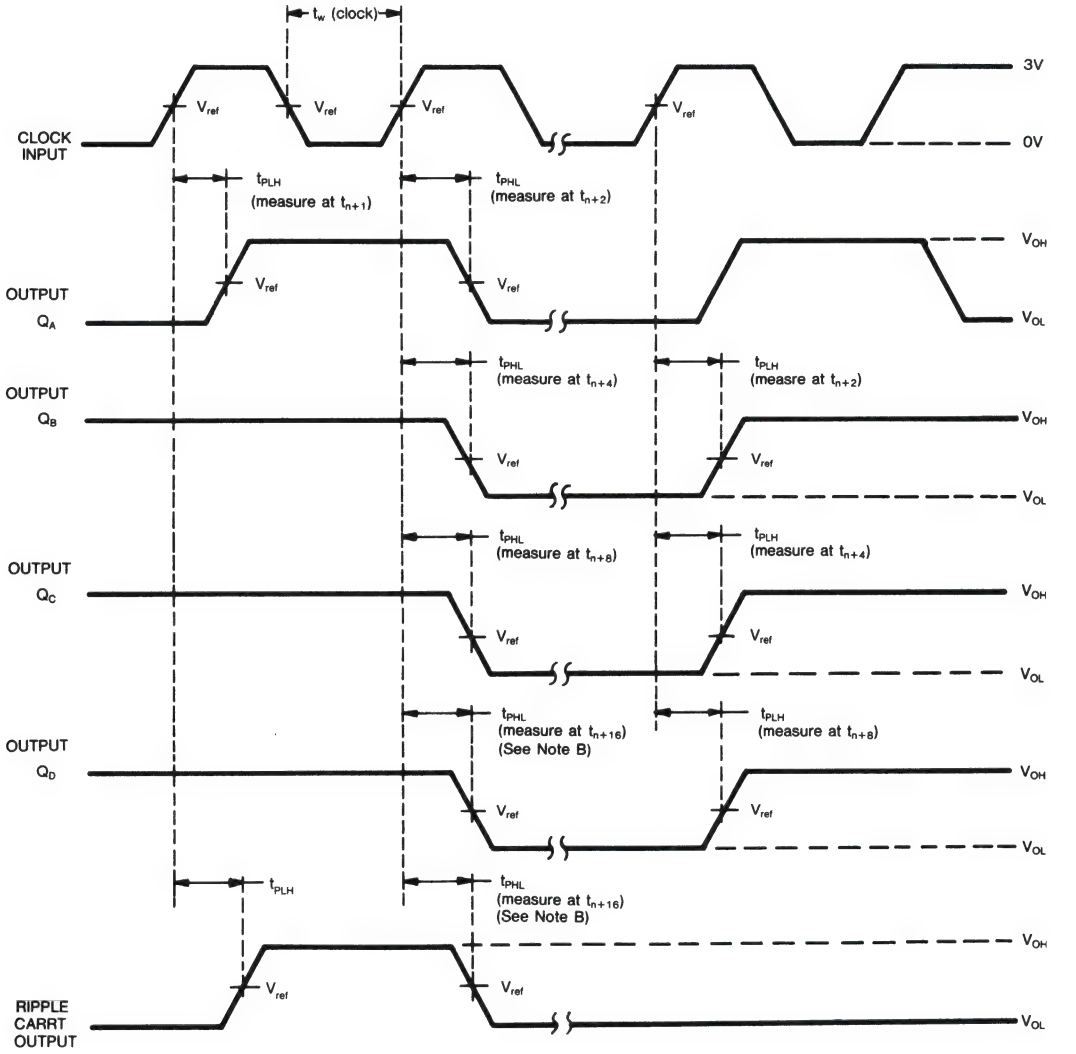
PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}			$C_L=15pF$, $R_L=2k\Omega$, See Note 1	25	32		MHz
t_{PLH}	Clock	Ripple carry			20	35	ns
t_{PHL}					18	35	
t_{PLH}	Clock (load input high)	Any Q			13	24	ns
t_{PHL}					18	27	
t_{PLH}	Clock (load input low)	Any Q			13	24	ns
t_{PHL}					18	27	
t_{PLH}	Enable T	Ripple carry			9	14	ns
t_{PHL}					9	14	
t_{PHL}	Clear	Any Q			20	28	ns

* f_{max} = maximum clock frequency
* t_{PLH} = propagation delay time, low-to-high-level output.
* t_{PHL} = propagation delay time, high-to-low-level output.
Note 1: propagation delay for clearing is measured from the clear input for the LS161A

Function Block Diagram

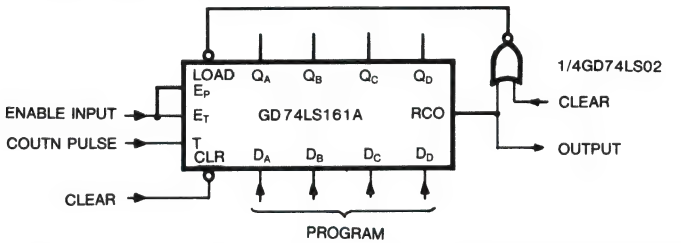


Parameter Measurement Information



Application Example

PROGRAMMABLE DIVIDER



D_A	D_B	D_C	D_D	Divide rate
L	L	L	L	1/16
H	L	L	L	1/15
L	H	L	L	1/14
H	H	L	L	1/13
L	L	H	L	1/12
H	L	H	L	1/11
L	H	H	L	1/10
H	H	H	L	1/9
L	L	L	H	1/8
H	L	L	H	1/7
L	H	L	H	1/6
H	H	L	H	1/5
L	L	H	H	1/4
H	L	H	H	1/3
L	H	H	H	1/2

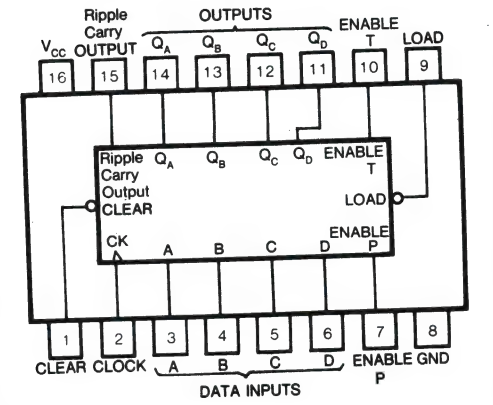
Note: Reset is performed by applying count pulse with reset input high $\overline{RD}$ pin can't be used since Q_A-Q_D should be set low.

GD54/74LS163A
SYNCHRONOUS
4-BIT COUNTER: BINARY, SYNCHRONOUS CLEAR

Feature

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

This synchronous, presettable counter features an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating.

This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input wave form.

This counter is fully programmable; that is the outputs may be preset to either level. As presetting is synchronous setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two counter-enable inputs and a ripple carry output. Both countenable inputs (ENABLE P and ENABLE T) must be high to count, and ENABLE T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high level portion of the Q_A output. The high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

Function Table (Note 1)

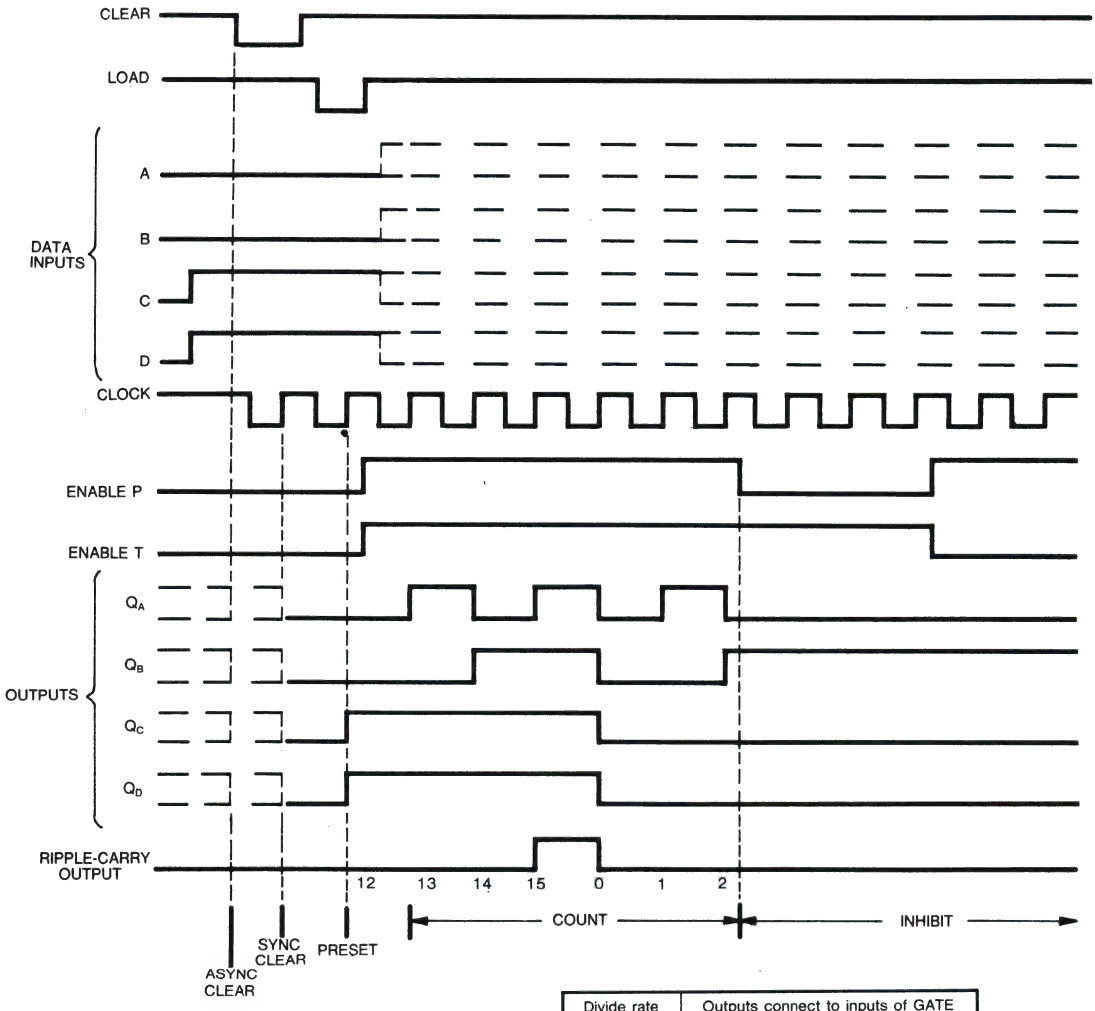
$\overline{CLR}$	$\overline{LOAD}$	E_T	E_P	CK	Q_A	Q_B	Q_C	Q_D	RCO
L	X	X	X	↑	L	L	L	L	L
H	L	L	X	↑	D_A	D_B	D_C	D_D	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Inhibit				L
H	H	H	L	X	Inhibit				L*

Note 1: ↑ : Indicates a transition from low to high (positive edge triggering).
* : RCO output is normally low-level, but RCO output is high-level when E_T input is high-level while the counter is in its maximum count state (HHHH).
X : irrelevant

Typical Clear, Preset, Count, and Inhibit Sequences

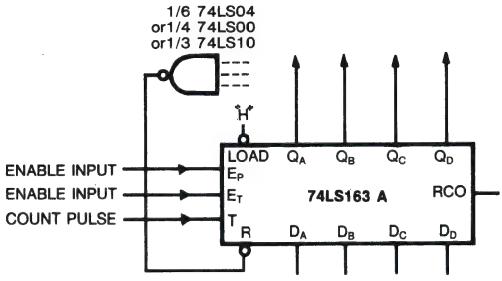
Illustrated below is the following sequence:

1. Clear outputs to zero synchronous
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit



Application Example

VARIABLE MODULO COUNTER



Divide rate	Outputs connect to inputs of GATE
3	Q_B
5	Q_C
6	Q_A, Q_C
7	Q_B, Q_C
9	Q_D
10	Q_A, Q_D
11	Q_B, Q_D
12	Q_A, Q_B, Q_D
13	Q_C, Q_D
14	Q_A, Q_C, Q_D
15	Q_B, Q_C, Q_D

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
f_{clock}	Clock frequency		0		25	MHz
$tw_{(clock)}$	Width of clock pulse		25			ns
$tw_{(clear)}$	Width of clear pulse		20			ns
t_{SU}	Setup time	Data inputs A,B,C,D.	20			ns
		Enable P or T	20			
		Load, Clear	20			
t_h	Hold time at any input		3			ns
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	Data or enable P				0.1	mA
			Load, clock or enable T				0.2	
			Clear				0.2	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	Data or enable P				20	μA
			Load, clock or enable T				40	
			Clear				40	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	Data or enable P				−0.4	mA
			Load, clock or enable T				−0.8	
			Clear				−0.8	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=Max (Note 3)				18	31	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=Max (Note 4)				18	32	mA

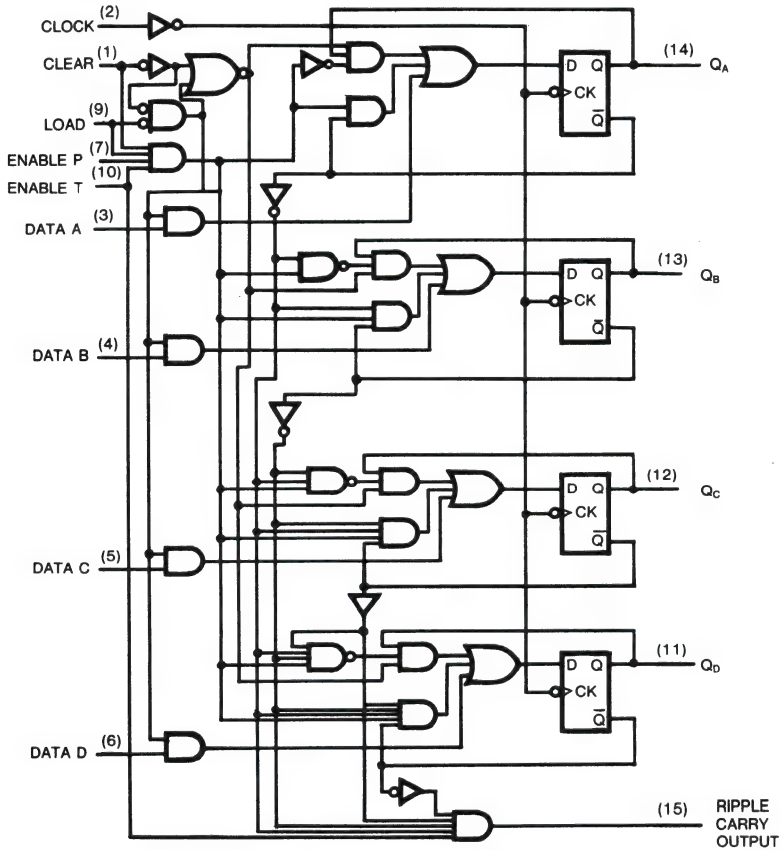
Note 1: All typicals are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.
Note 4: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}			$C_L=15pF$, $R_L=2k\Omega$, See Note 1	25	32		MHz
t_{PLH}	Clock	Ripple carry			20	35	ns
t_{PHL}					18	35	
t_{PLH}	Clock (load input high)	Any Q			13	24	ns
t_{PHL}					18	27	
t_{PLH}	Clock (load input low)	Any Q			13	24	ns
t_{PHL}					18	27	
t_{PLH}	Enable T	Ripple carry			9	14	ns
t_{PHL}					9	14	
t_{PHL}	Clear	Any Q			20	28	ns

* f_{max} = maximum clock frequency
* t_{PLH} = propagation delay time, low-to-high-level output.
* t_{PHL} = propagation delay time, high-to-low-level output.
Note 1: propagation delay for clearing is measured from the clock transition for the LS163A.

Function Block Diagram



GD54/74LS164

8-BIT PARALLEL OUTPUT SERIAL SHIFT REGISTER

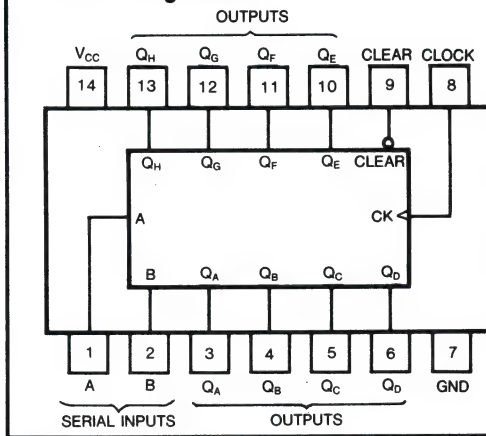
Feature

- Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear

Description

This 8-bit shift register features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip flop to the low level at the next clock pulse. A high level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered clocking occurs or the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

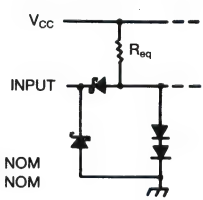
Function Table

INPUTS				OUTPUTS	
CLEAR	CLOCK	A	B	Q_A	$Q_B \cdots Q_H$
L	X	X	X	L	L ··· L
H	L	X	X	Q_{AO}	$Q_{BO} \cdots Q_{HO}$
H	↑	H	H	H	$Q_{Gn} \cdots Q_{Gn}$
H	↑	L	X	L	$Q_{An} \cdots Q_{Gn}$
H	↑	X	L	L	$Q_{An} \cdots Q_{Gn}$

H=high level (steady state), L=low level (steady state)
X=irrelevant (any input, including transitions)
↑=transition from low-to-high-level
Q_{AO}, Q_{BO}, Q_{HO}=the level of Q_A, Q_B or Q_H respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn}=the level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

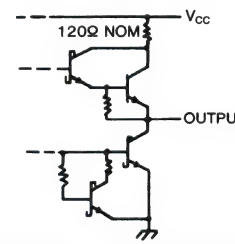
Schematics of Inputs and Outputs

EQUIVALENT OF EACH INPUT

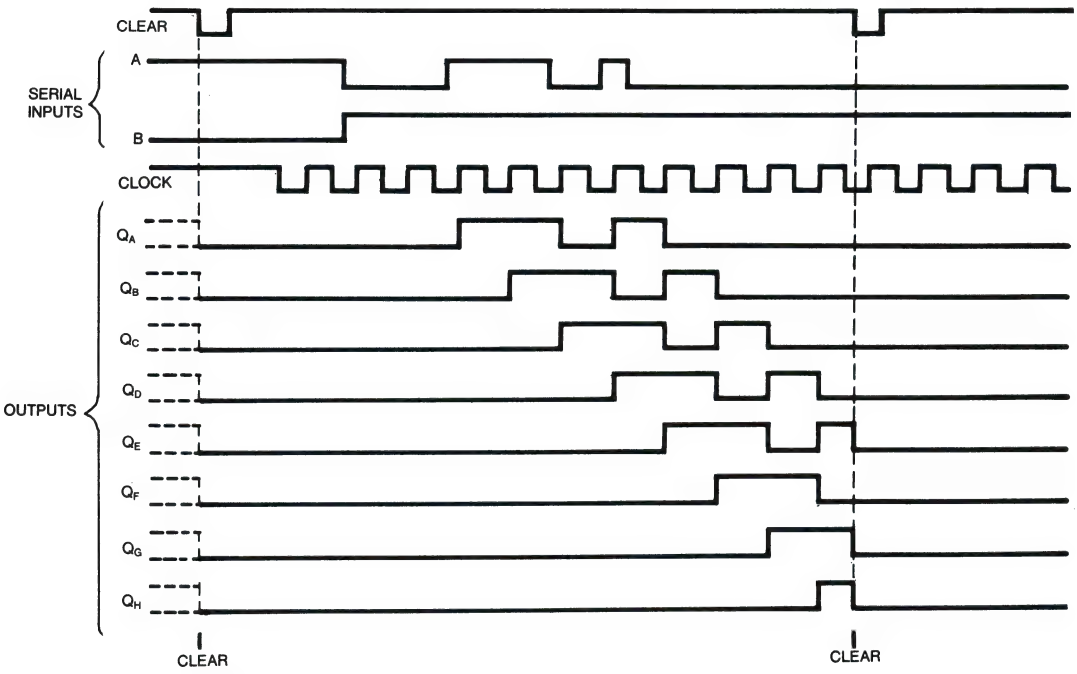


CLEAR, CLOCK: 17KΩ NOM
SERIAL: 25KΩ NOM

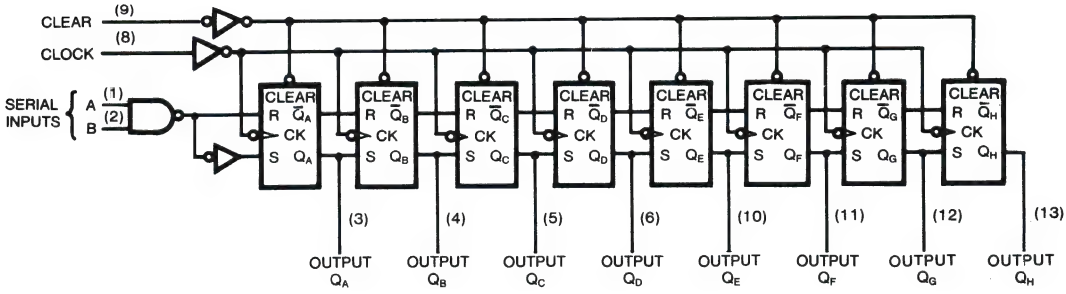
TYPICAL OF ALL OUTPUTS



Typical Clear, Shift, and Clear Sequences



Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
f_{clock}	Clock frequency		0		25	MHz
t_w	Width of clock or clear input pulse		20			ns
t_{su}	Data set up time		15			ns
t_h	Data hold time		5			ns
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min	V_{IL}=Max	54	2.5	3.4		V
		I_{OH}=Max	V_{IH}=Min	74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	mA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 3)				16	27	mA

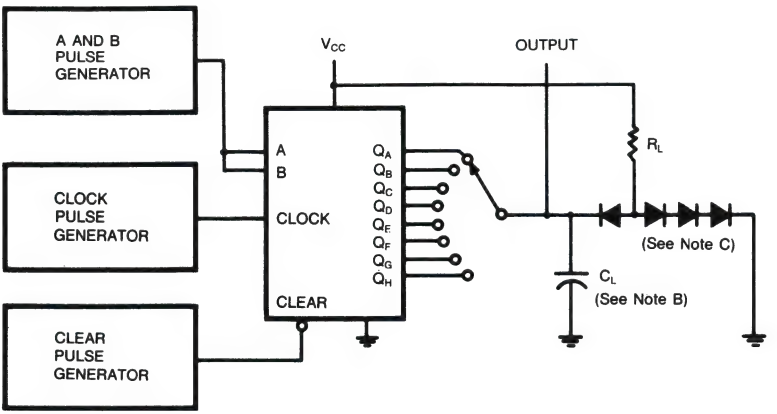
Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
Note 3: I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4V, and a momentary ground, then 4.5V applied.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

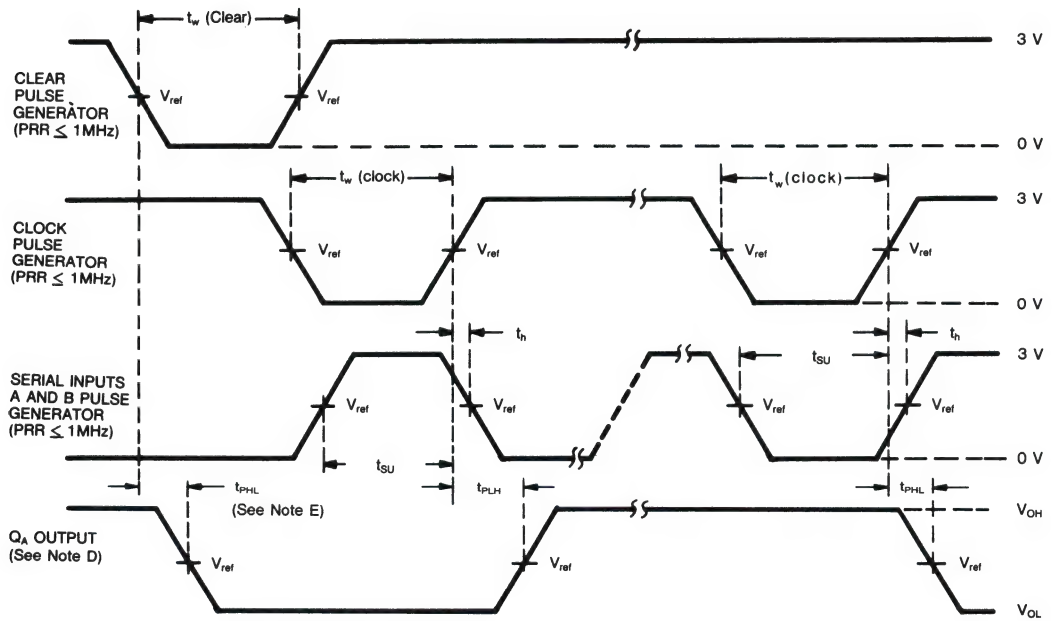
SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency		25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input	$C_L=15pF$, $R_L=2k\Omega$ See Figure 1		24	36	ns
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input			17	27	ns
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input			21	32	ns

#For load circuit and voltage waveforms, see page 3-11.

Parameter Measurement Information



TEST CIRCUIT



VOLTAGE WAVEFORMS

Note A: The pulse generators have the following characteristics: duty cycle ≤50%, $Z_{out} \approx 50\Omega$; $t_r \leq 15$ns, $t_f \leq 6$ns.
Note B: C_L includes probe and jig capacitance.
Note C: All diodes are 1N3064 or 1N916
Note D: Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
Note E: Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.
Note F: $V_{ref} = 1.3V$

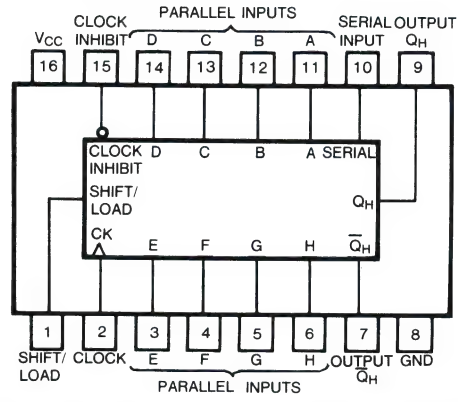
Figure 1 Switching Times

GD54/74LS165
PARALLEL-LOAD 8-BIT SHIFT REGISTERS WITH COMPLEMENTARY OUTPUTS

Feature

- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

This device is 8 bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eight bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input independently of the levels of the clock, clock inhibit, or serial inputs.

Function Table

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{AO}	Q_{BO}	Q_{HO}

H=High Level (steady state), L=Low Level (steady state) X=Irrelevant (any input, including transitions) ↑ =Transition from low to high level a...h=The level of steady-state input at inputs A through H, respectively Q_{AO}, Q_{BO}, Q_{HO}=The level of Q_A, Q_B, Q_H, respectively, before the indicated steady-stae input conditions were established Q_{An}, Q_{Gn}=The level of Q_A, Q_G, respectively, before the most recent ↑ transition of the clock.

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54,74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{clock}	Clock frequency			0		25	MHz
t_W	Pulse Width	Clock		25			ns
		Load		15			
t_{SU}	Setup Time	Parallel		10			ns
		Serial		20			
		Enable		30			
		Shift		45			
t_H	Hold Time			0			ns
T_A	Operating free-temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−12mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IH}=Min I_{OH}=Max V_{IL}=Max		54	3.5	2.5		V
				74	2.7	3.5		
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	Shift/load				0.3	mA
			Other inputs				0.1	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	Shift/load				60	μA
			Other inputs				20	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	Shift/load				−1.2	mA
			Other inputs				−0.4	
I_{OS}	Short-circuit output current	V_{CC}=5.25V (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				18	30	mA

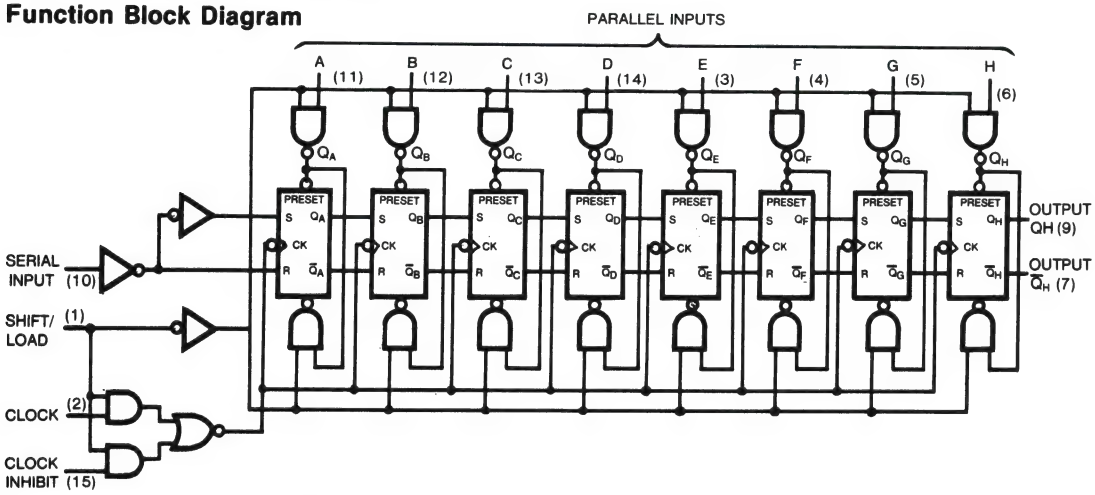
Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
Note 3: With all outputs open, clock inhibit and shift/load at 4.5V, and a clock pulse applied to the CLOCK input, I_{CC} is measured first with the parallel inputs at 4.5V, then again grounded.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

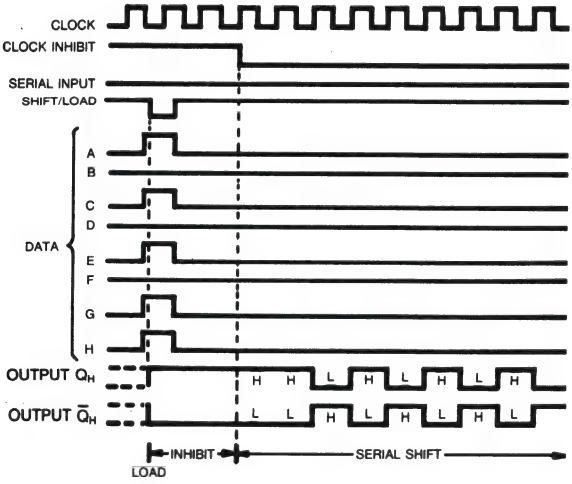
PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}			$C_L=15pF$, $R_L=2k\Omega$ See Fig 1-3.	25	35		MHz
t_{PLH}	Load	Any			21	35	ns
t_{PHL}					26	35	ns
t_{PLH}	Clock	Any			14	25	ns
t_{PHL}					16	25	
t_{PLH}	H	Q_H			13	25	ns
t_{PHL}					24	30	
t_{PLH}	H	$\overline{Q}_H$			19	30	ns
t_{PHL}					17	25	

* f_{max} = maximum clock frequency.
t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output.

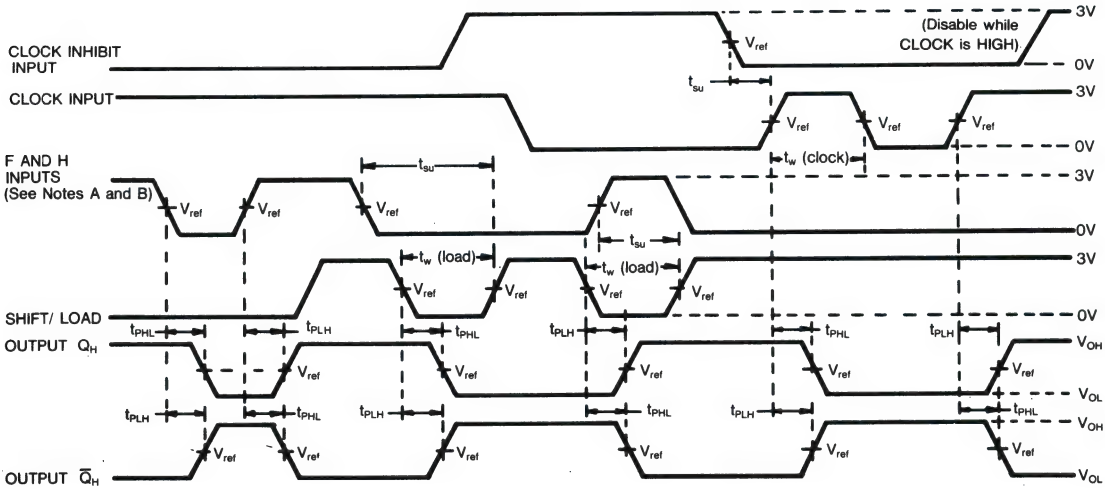
Function Block Diagram



Typical Shift, Load, and Inhibit Sequences

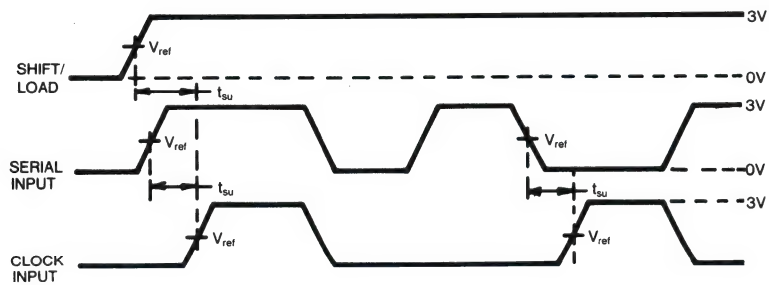


Parameter Measurement Information



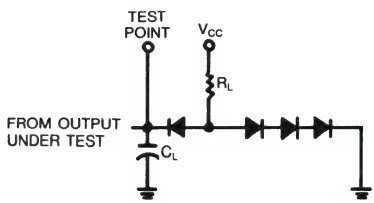
Notes: A. The remaining six data inputs and the serial input are low.
B. Prior to test, high-level data is loaded into H input.
C. The input pulse generators have the following characteristics: PRR≤1MHz, duty cycle≤50% Z_{out}≈50Ω; t_r≤15ns. t_f≤6ns.
D. V_{ref}=1.3V.

Figure 1-Voltage Waveforms



Notes: A. The eight data inputs and the clock-inhibit input are low. Results are monitored at output Q_H at t_{n+7}.
B. The input pulse generators have the following characteristics PRR≤1MHz, duty cycle≤50%, Z_{out}≈50Ω; t_r≤15ns, t_f≤6ns.
C. V_{ref}=1.3V

Figure 2-Voltage Waveforms



Notes: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.

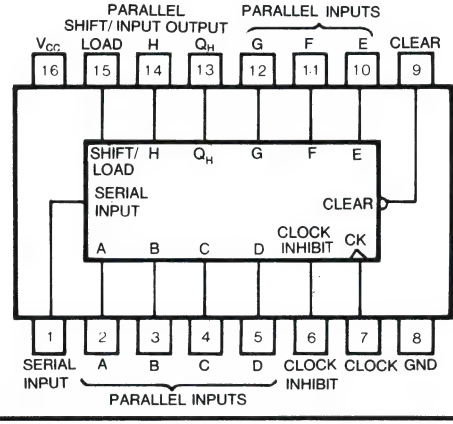
Figure 3-Load Circuit for Switching Tests

GD54/74LS166
8-BIT SHIFT REGISTERS PARALLEL/ SERIAL INPUT SERIAL OUTPUT

Feature

- Synchronous Load
- Direct Overriding Clear
- Parallel to Serial Conversion

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

This 8-bit shift register is compatible with most other TTL and DTL logic families. All inputs are buffered to lower the drive requirements. Input clamping diodes minimize switching transients and simplify system design.

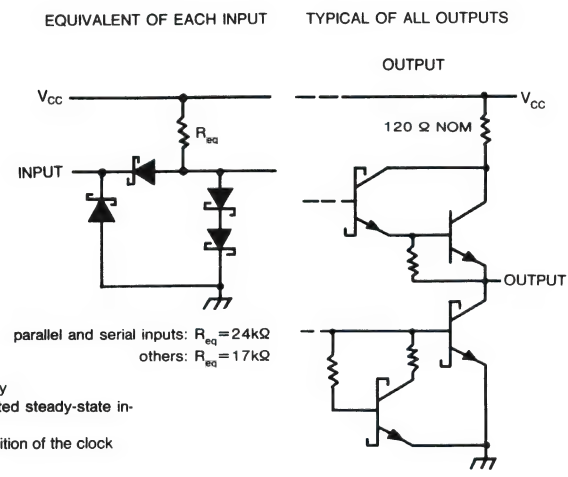
These parallel-in or serial-in, serial-out shift registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking, holding either low enables the other clock input. This of course, allows the system clock to be free-running and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs including the clock, and sets all flip-flops to zero.

Function Table

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A H	Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{AO}	Q_{BO}	Q_{HO}

H=High Level (steady state). L=Low Level (steady state)
X=Don't Care (any input, including transitions)
↑=Transition from low to high level
a...h=The level of steady-state input at inputs A through H, respectively
Q_{AO}, Q_{BO}, Q_{HO}=The level of Q_A, Q_B, Q_H, respectively before the indicated steady-state input conditions were established
Q_{An}, Q_{Gn}=The level of Q_A, Q_G respectively, before the most recent ↑ transition of the clock

Schematics of Inputs and Outputs



parallel and serial inputs: R_{eq}=24kΩ
others: R_{eq}=17kΩ

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
f_{clock}	Clock frequency		0		25	MHz
t_{su}	Mode-control set up time		30			ns
t_w	Width of clock or clear pulse		20			ns
t_h	Data hold time		0			ns
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.7	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max	54	2.5	3.4		V
		I_{OH}=Max, V_{IH}=Min	74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min, I_{OL}=4mA	54,74		0.25	0.4	V
		V_{CC}=Min, V_{IL}=Max, V_{IH}=Min, I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)			20	32	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
Note 3: With all outputs open, 4.5V applied to the serial input, all other inputs except the CLOCK grounded, I_{CC} is measured after a momentary ground, then 4.5V, is applied to the CLOCK.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	$C_L=15pF$, $R_L=2k\Omega$ See Figure 3	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level outputs from clear			19	30	ns
t_{PHL}	Propagation delay time, high-to-low-level outputs from clock		7	14	25	ns
t_{PLH}	Propagation delay time, low-to-high-level outputs from clock		5	11	20	ns

Function Block Diagram

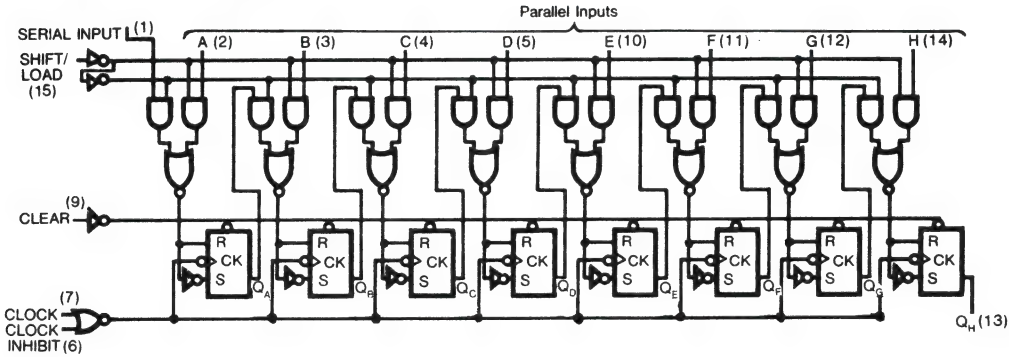


Figure 1.

Typical Clear, Shift, Load, Inhibit, and Shift Sequences

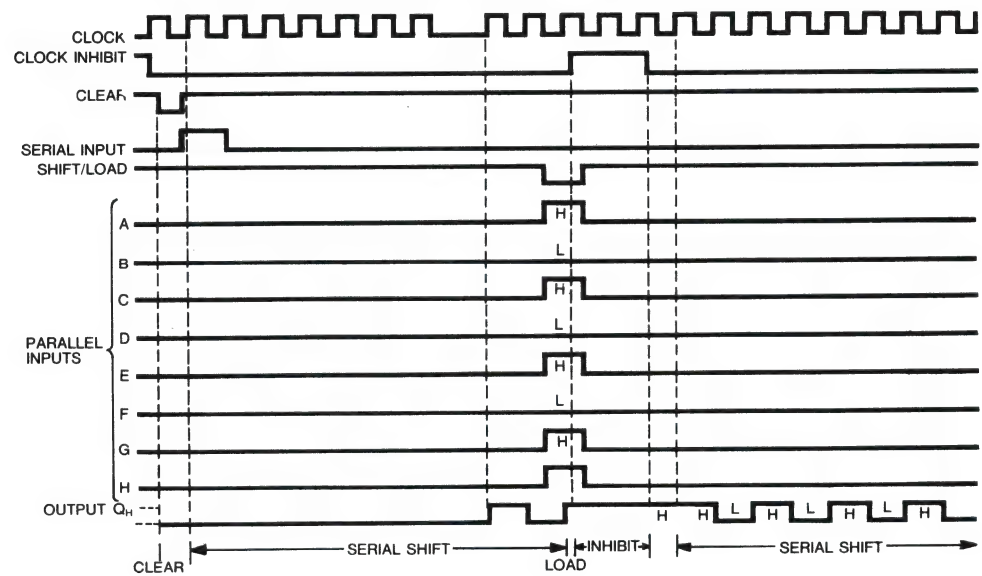
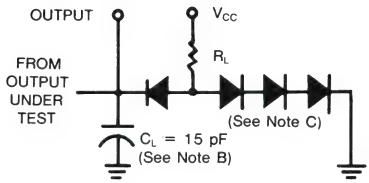


Figure 2.

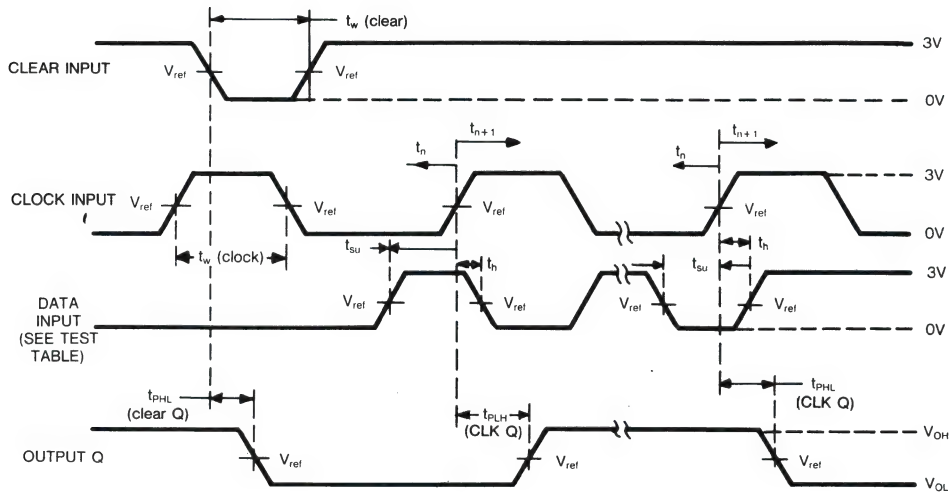
Parameter Measurement Information



LOAD FOR OUTPUT UNDER TEST

Test Table for Synchronous Inputs

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTEF)
H	0V	Q_H at t_{n+1}
Serial Input	4.5V	Q_H at t_{n+8}



VOLTAGE WAVEFORMS

Figure 3.

Notes: A. All pulse generators have the following characteristics; Z_{out}≈50Ω, tr≤15ns and t_f≤6ns.
B. The clock pulse has the following characteristics; t_w (clock)≤20ns and PRR=1MHz. The clear pulse has the following characteristics; t_w(clear)≥20ns and t_{hold}=0ns, when testing $f_{max.}$ vary the clock PRR.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064 or 1N916.
E. A clear pulse is applied prior to each test.
F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.
G. t_n=bit time before clocking transistion.
t_{n+1}=bit time after one clocking transition.
t_{n+8}=bit time after eight clocking transition.
H. V_{ref}=1.3V.

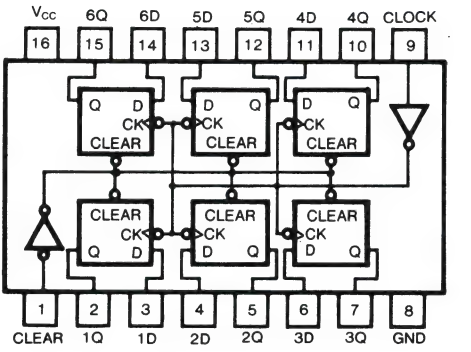
GD54/74LS174

HEX D-TYPE FLIP-FLOPS, COMMON CLEAR

Feature

- Contains Six Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Application Include: Buffer/Storage Registers
  Shift Registers
  Pattern Generators

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

These monolitic, positive-edge triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic.

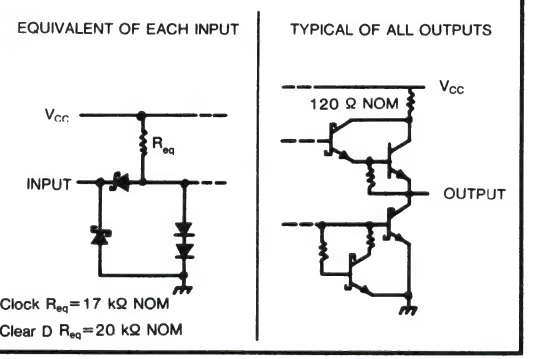
Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Function Table (Each F/F)

INPUTS			OUTPUTS
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑*	H	H
H	↑*	L	L
H	L	X	Q_0^*

*↑=transition from low to high level.
*Q_0=the level of Q before the indicated steady-state input conditions were established.

Schematics of Inputs and Outputs



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54,74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{clock}	Clock frequency			0		30	MHz
t_w	Width of clock or clear pulse			20			ns
t_{su}	Set up time	Data input		20			ns
		Clear inactive-state		25			
t_h	Data hold time			5			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V, (Note 3)				16	26	mA

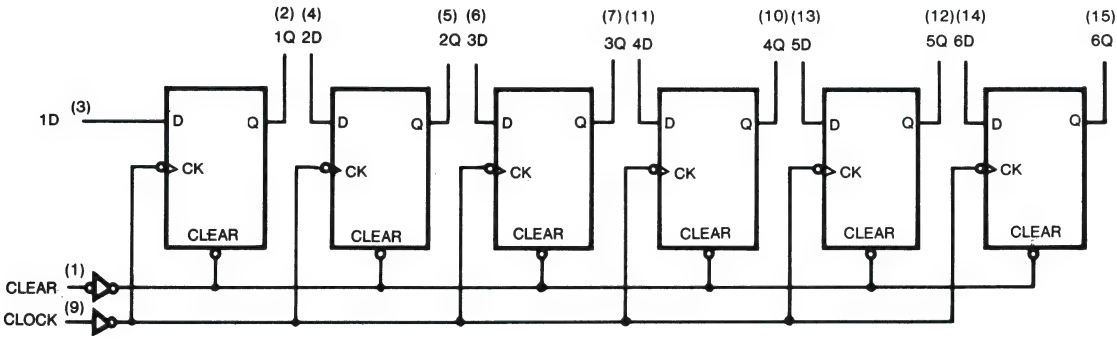
Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
Note 3: With all outputs open, 4.5V applied to the serial input, all other inputs except the CLOCK grounded, I_{CC} is measured after a momentary ground, then 4.5V, is applied to the CLOCK.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L=15pF, R_L=2kΩ	30	40		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	30	ns

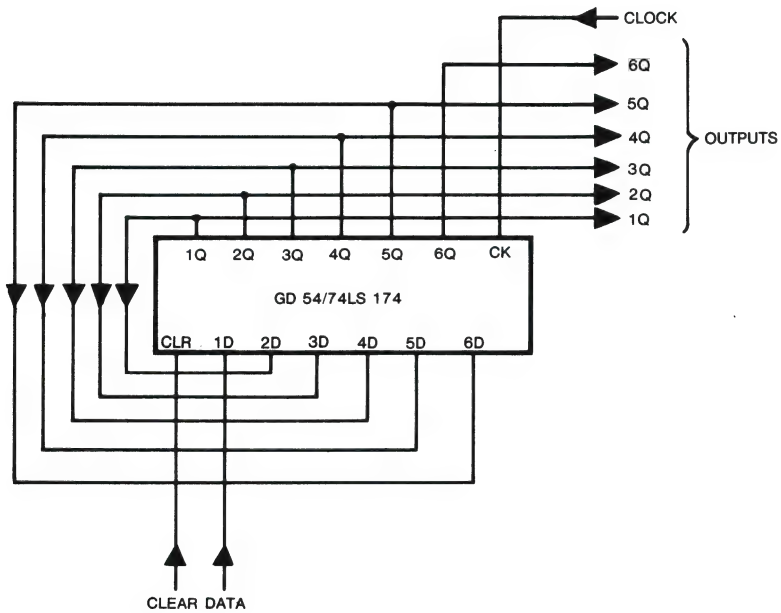
#For load circuit and voltage waveforms, see page 3-11.

Function Block Diagram



Application Example

(6-BIT SHIFT REGISTER)



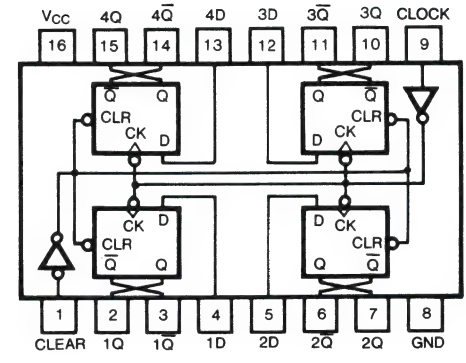
GD54/74LS175

QUAD D-TYPE FLIP-FLOPS

Feature

- Contains Four Flip-Flops with Double-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications: Buffer/Storage Registers
  Shift Registers
  Pattern Generators

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

This monolithic, positive edge-triggered flip-flops utilize, TTL circuitry to implement D-type flip-flop logic.

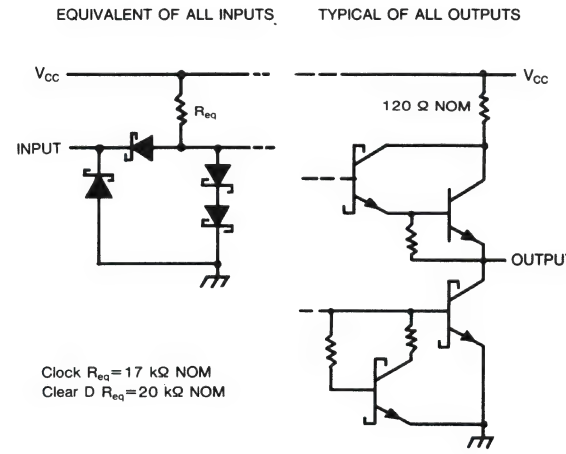
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Function Table

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑*	H	H	L
H	↑*	L	L	H
H	L	X	Q_{O^*}	$\overline{Q}_O$

*↑=transition from low to high level.
*Q_O=the level of Q before the indicated steady-state input conditions were established.

Schematics of Inputs and Outputs



Clock R_{eq}=17 kΩ NOM
Clear D R_{eq}=20 kΩ NOM

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54,74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{clock}	Clock frequency			0		30	MHz
t_w	Width of clock or clear pulse			20			ns
t_{su}	Set up time	Data input		20			ns
		Clear inactive-state		25			
t_h	Data hold time			5			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V, (Note 3)				11	18	mA

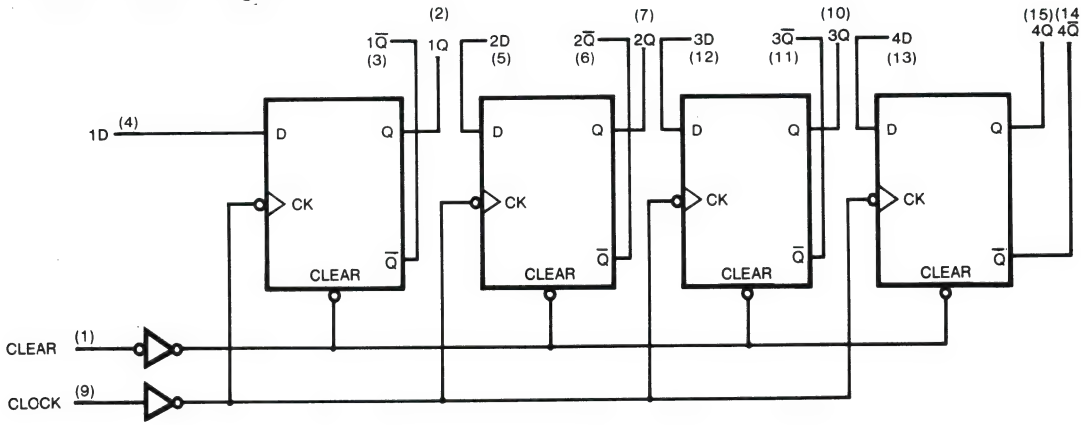
Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
Note 3: With all outputs open and 4.5V applied to all data and clear inputs. I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	$C_L=15pF$, $R_L=2k\Omega$	30	40		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			13	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			16	25	ns

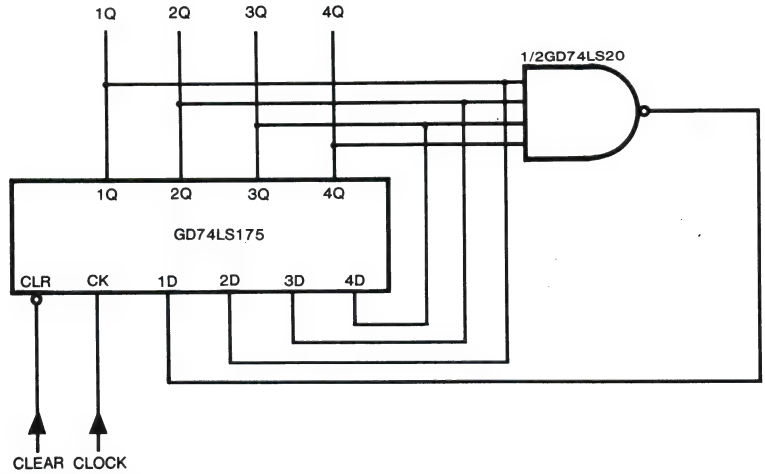
For load circuit and voltage waveforms, see page 3-11.

Function Block Diagram



Application Example

TIMING PULSE GENERATOR



GD54/74LS191
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS WITH MODE CONTROL

Features

- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n-bit applications
- Average propagation delay 20 ns
- Typical clock frequency 25 MHz
- Typical power dissipation 100mW

Description

These circuits are synchronous, reversible, up/down counters. The LS191 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

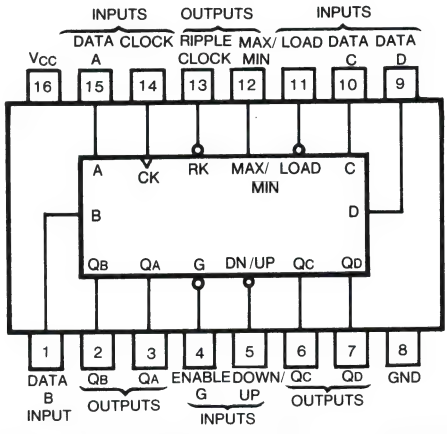
The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The later output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

$\overline{LOAD}$	$\overline{G}$	$\overline{DN}$/UP	CK	QA	QB	QC	QD
L	X	X	X	DA	DB	DC	DD
H	L	L	↑	Count Up			
H	L	H	↑	Count Down			
H	H	X	X	Inhihit			

$\overline{G}$	MAX/ MIN *	CK	RK
L	H	L	L
L	H	H	H
H	X	X	H
X	L	X	H

* Min/Max is output but the signal generated internally the following logical expression

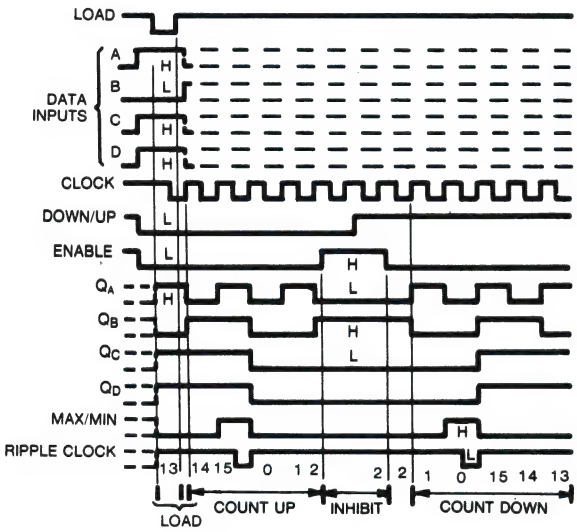
Count up...Min/Max=$Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot (\overline{DN}/UP)$

Count down...Min/Max=$\overline{Q}_A \cdot \overline{Q}_B \cdot \overline{Q}_C \cdot \overline{Q}_D \cdot (\overline{DN}/UP)$

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

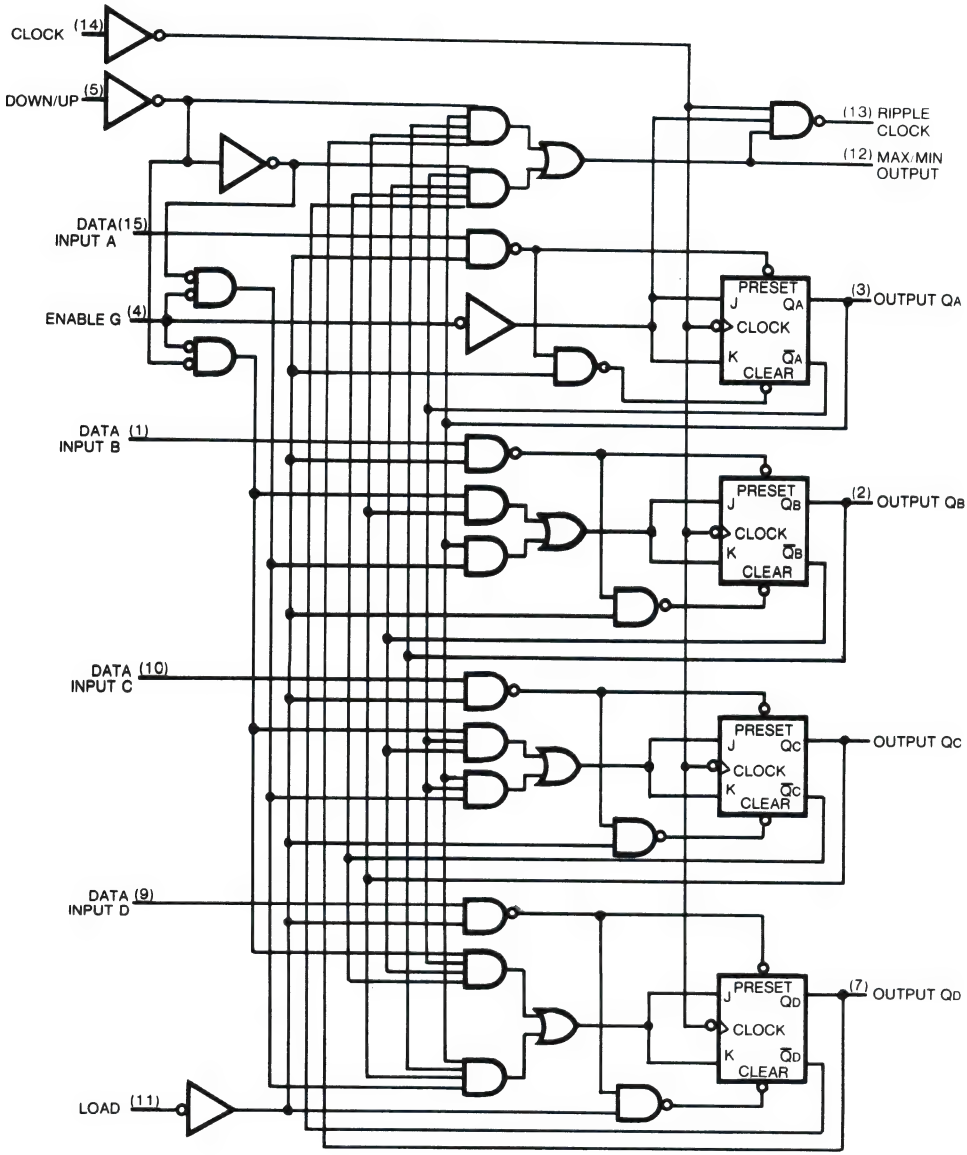
LS191 Binary Counters
Typical Load, Count, and Inhibit Sequences



Sequence:
(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen, and thirteen

Function Block Diagram

LS191 Binary Counters



Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54,74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{clock}	Clock frequency			0		20	MHz
t_W	Pulse width	Clock		25			ns
		Load		35			
t_{su}	Data setup time			20			ns
t_h	Data hold time			5			ns
t_{EN}	Enable time to clock			40			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
		I_{OH}=Max, V_{IH}=Min		74	2.7	3.4		
V_{OL}	Low level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	Enable				0.3	mA
			Others				0.1	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	Enable				60	μA
			Others				20	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	Enable				−1.2	mA
			Others				−0.4	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				25	35	mA

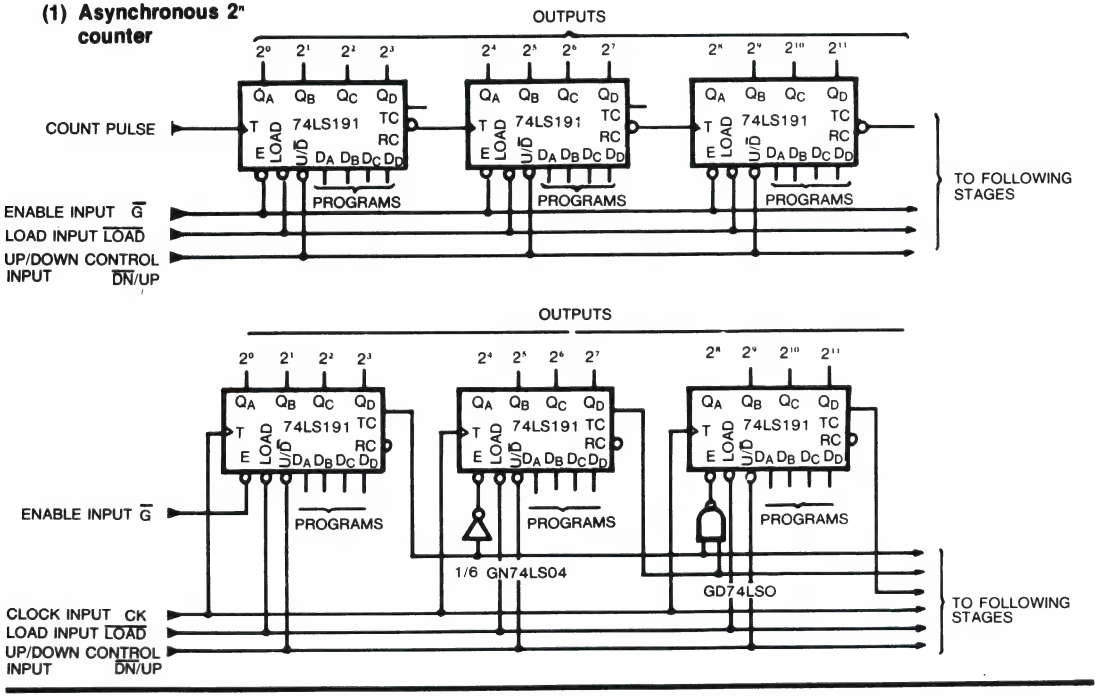
Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM(INPUT)	TO(OUTPUT)	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}				20	25		MHz
t_{PLH}	Load	Any Q	$C_L=15pF$ $R_L=2k\Omega$ See Note 1		22	33	ns
t_{PHL}					33	50	
t_{PLH}	Data	Any Q			20	32	ns
t_{PHL}					27	40	
t_{PLH}	Clock	Ripple Clock			13	20	ns
t_{PHL}					16	24	
t_{PLH}	Clock	Any Q			16	24	ns
t_{PHL}					24	36	
t_{PLH}	Clock	Max/Min			28	42	ns
t_{PHL}					37	52	
t_{PLH}	Down/Up	Ripple Clock			30	45	ns
t_{PHL}					30	45	
t_{PLH}	Down/Up	Max/Min			21	33	ns
t_{PHL}					22	33	
t_{PLH}	Enable	Ripple Clock			21	33	ns
t_{PHL}					22	33	

Application Examples

(1) Asynchronous 2" counter



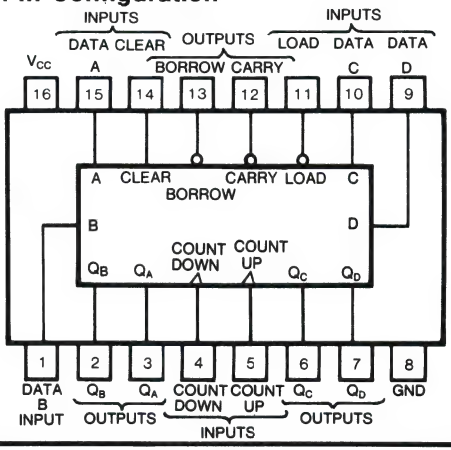
GD54/74LS193

SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS;BINARY WITH CLEAR

Feature

- Cascading Circuitry Provided Internally
- Synchronous Operation
- Individual Preset to Each Flip-Flop
- Fully Independent Clear Input

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

The LS193 is synchronous, reversible up/down counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs, change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuit. Both borrow and carry outputs are available to cascade both the up-and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

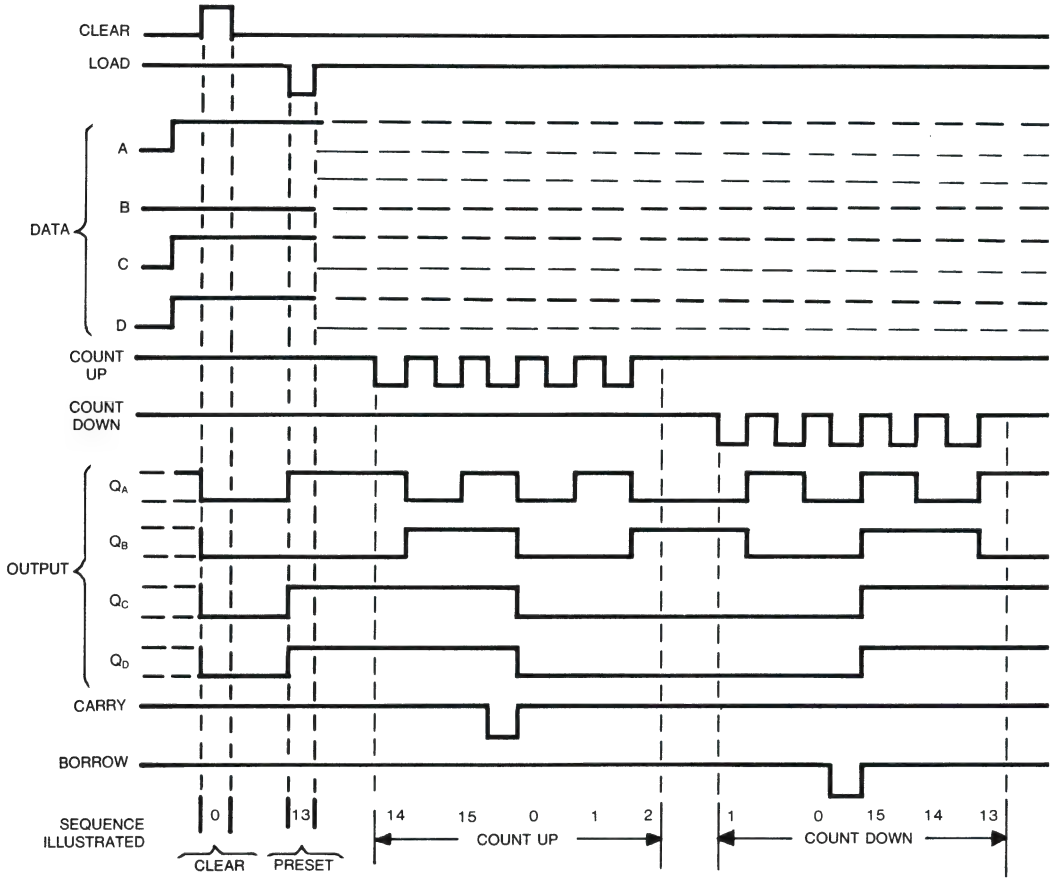
FUNCTION TABLE

INPUTS								OUTPUTS						CONDITIONS
Clock		Data												
Up	Down	Clear	Load	A	B	C	D	Q_A	Q_B	Q_C	Q_D	Borrow	Carry	
X	L	H	X	X	X	X	X	L	L	L	L	L	H	Clear
X	H	H	X	X	X	X	X	L	L	L	L	H	H	
X	X	L	L	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3	X	X	Load
H	↑	L	H	X	X	X	X	Count Down				H	H	Except at borrow
H	L	L	H	X	X	X	X	L	L	L	L	L	H	Borrow
H	H	L	H	X	X	X	X	L	L	L	L	H	H	
↑	H	L	H	X	X	X	X	Count up				H	H	Except at carry
L	H	L	H	X	X	X	X	H	H	H	H	H	L	Carry
H	H	L	H	X	X	X	X	H	H	H	H	H	H	

Typical Clear, Load, and Count Sequences

Illustrated below is the following sequence:

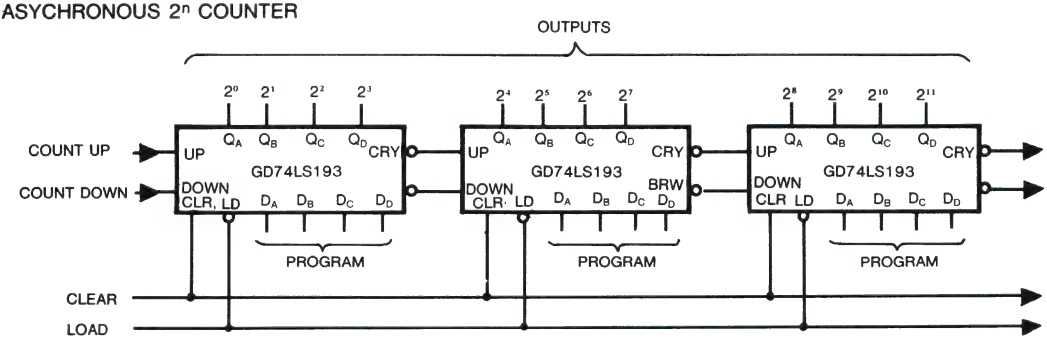
1. Clear outputs to zero
2. Load (preset) to binary thirteen
3. Count up to fourteen, fifteen, carry, zero, one, and two
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



Notes: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high, when counting down, count-up input must be high.

Application Example

ASYNCHRONOUS 2^n COUNTER



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
f_{clock}	Clock frequency		0		25	MHz
t_w	Width of any input pulse		20			ns
t_{su}	Clear inactive-state set up time		40			ns
t_{th}	Data hold time		5			ns
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V, (Note 3)				19	34	mA

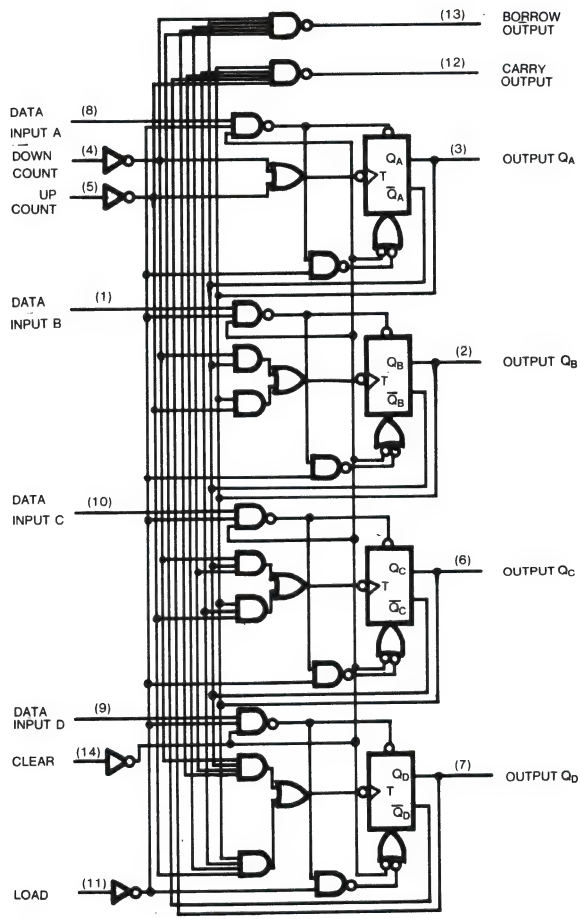
Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
Note 3: I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5V.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

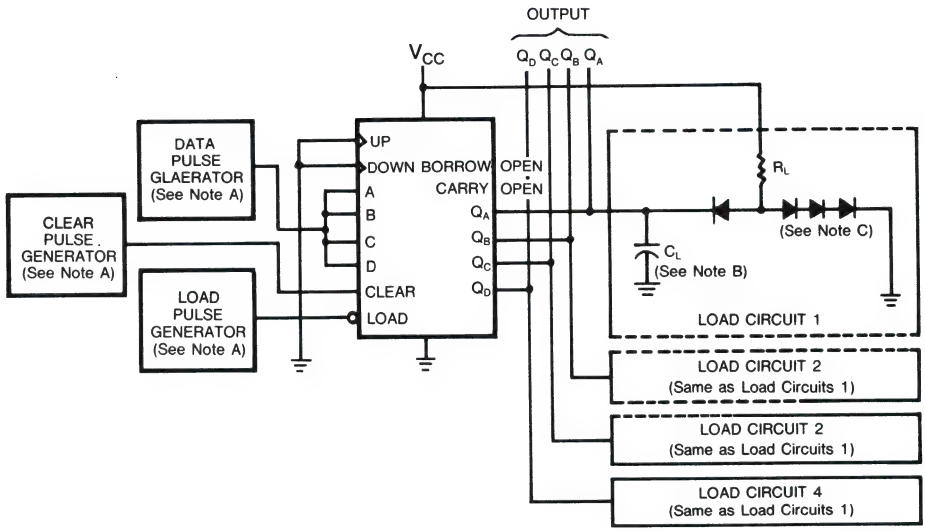
PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CIBDITION	MIN	TYP	MAX	UNIT
f_{max}			$C_L=15pF$, $R_L=2k\Omega$ See Figure 1 and 2	25	32		MHz
t_{PLH}	Coutn up	Carry			17	26	ns
t_{PHL}					18	24	
t_{PLH}	Count down	Borrow			16	24	ns
t_{PHL}					15	24	
t_{PLH}	Either Count	Q			27	38	ns
t_{PHL}					30	47	
t_{PLH}	Load	Q			24	40	ns
t_{PHL}					25	40	
t_{PHL}	Clear	Q			23	35	ns

* f_{max}=maximum clock frequency.
t_{PLH}=propagation delay time, low-to-high-level output
t_{PHL}=propagation delay time, high-to-low-level output

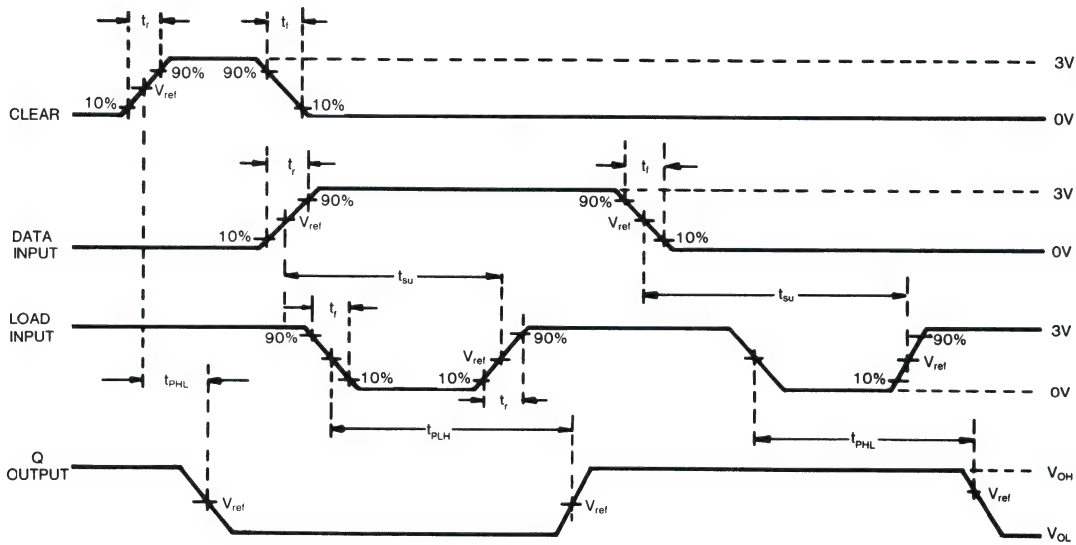
Function Block Diagram



Parameter Measurement Information



TEST CIRCUIT



VOLTAGE WAVEFORMS

Notes: A. The pulse generators have the following characteristics; $Z_{out} \approx 50\Omega$ and for the data pulse generator PRR $\leq$ 500kHz, duty cycle = 50%, for the load pulse generator PRR is two times data PRR, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064
D. t_r and $t_f \leq 7$ ns
E. v_{ref} is 1.3 volts

Figure 1. Clear Load and Set Up Times

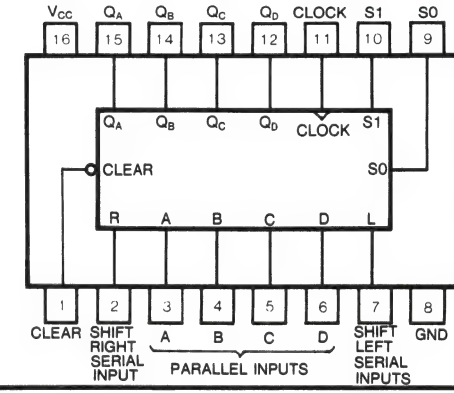
GD54/74LS194A

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

Feature

- Parallel Inputs and Outputs
- Four Operating Modes;
  Synchronous Parallel Load
  Right Shift
  Left Shift
  Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overding Clear

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear and outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Function Table

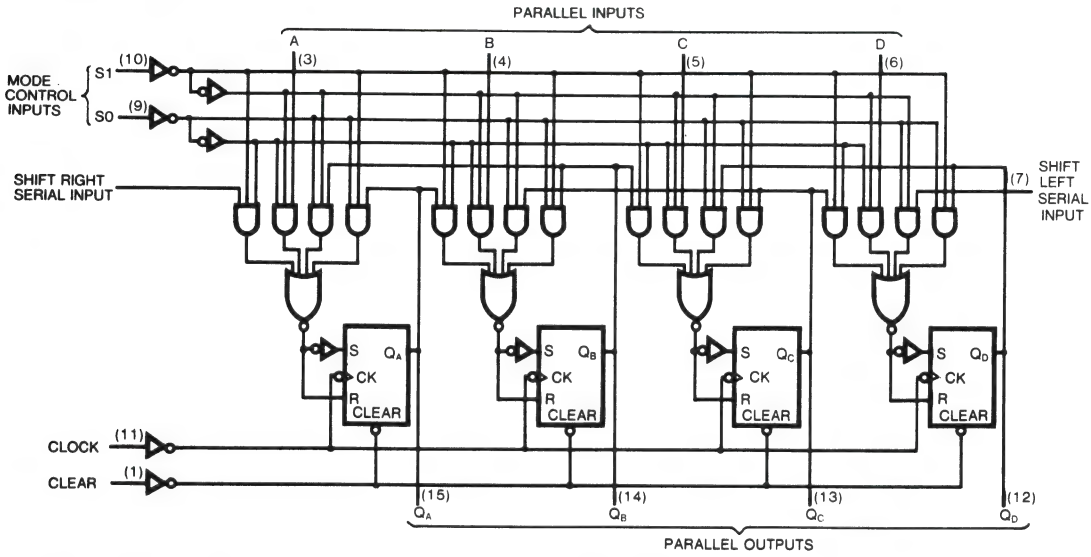
INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}

H=high level (steady state)
L=low level (steady state)
X=irrelevant (any input, including transitions)
↑=transition from low to high level
a,b,c,d=the level of steady state input at inputs A, B, C, or D, respectively.
Q_{AO}, Q_{BO}, Q_{CO}, Q_{DO}=the level of Q_A, Q_B, Q_C or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}=the level of Q_A, Q_B, Q_C or Q_D respectively, before the mostrecent ↑ transition of the clock.

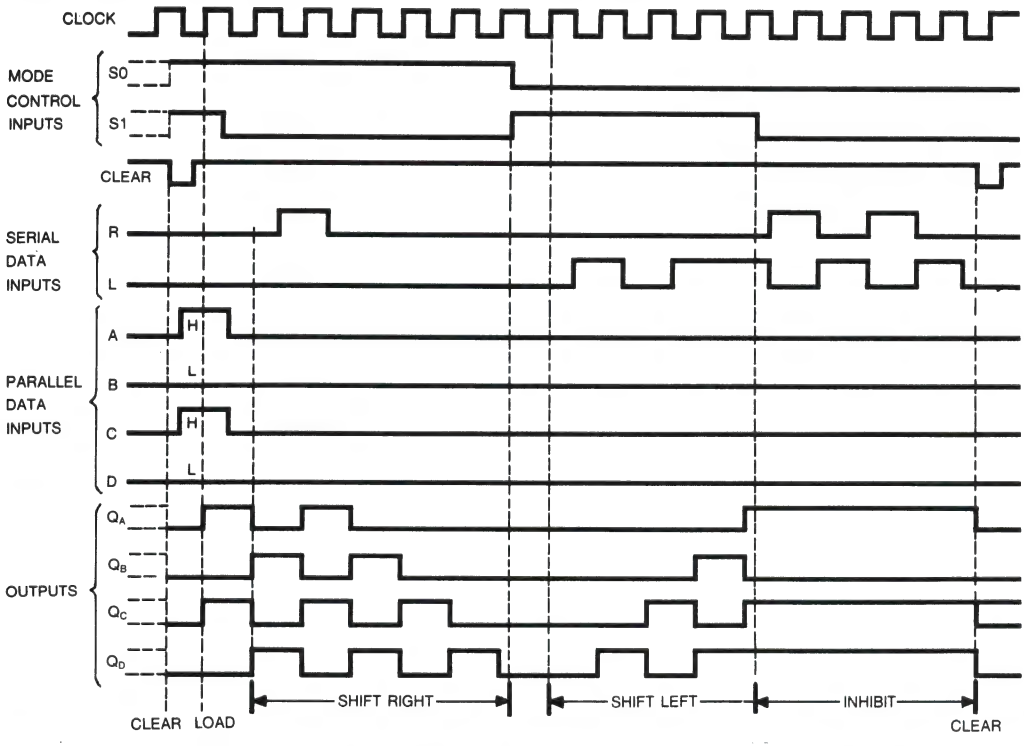
Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Function Block Diagram



Typical Clear, Load, Right-Shift, Inhibit, and Clear Sequences.



Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
f_{clock}	Clock frequency		0		25	MHz
t_w	Width of clock or clear pulse		20			ns
t_{su}	Set up time	Mode control	30			ns
		Serial and parallel data	20			ns
		Clear inactive-state	25			
t_h	Hold time at any input		0			ns
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

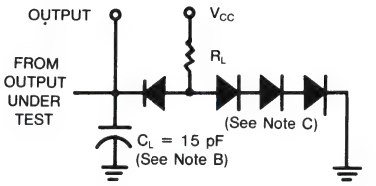
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V, (Note 3)				15	23	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
Note 3: With all outputs open and 4.5V applied to all data and clear inputs. I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L=15pF, R_L=2kΩ See Figure 1	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high level outputs from clock			14	22	ns
t_{PHL}	Propagation delay time, high-to-low level output from clock			17	26	ns

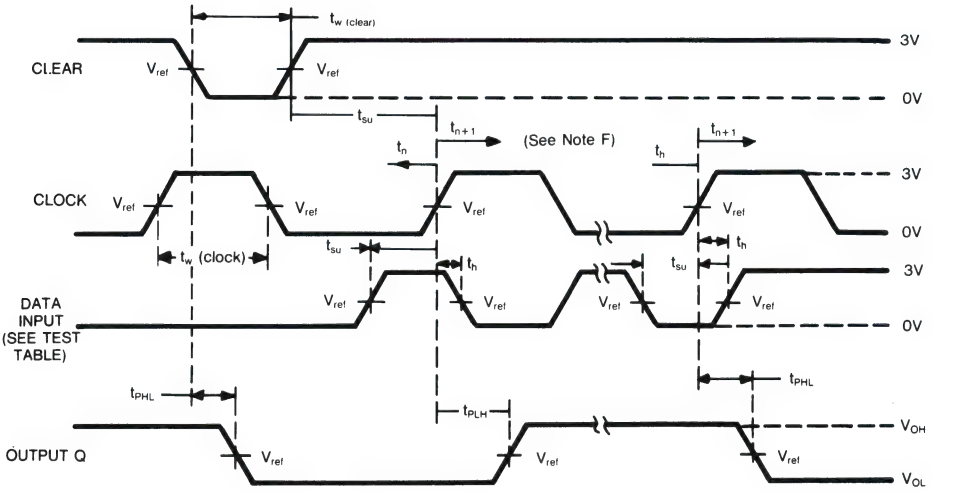
Parameter Measurement Information



LOAD FOR OUTPUT UNDER TEST

Test Table for Synchronous Inputs

Data Input For Test	S1	S0	Output Tested (See Note E)
A	4.5V	4.5V	Q_A at t_{n+1}
B	4.5V	4.5V	Q_B at t_{n+1}
C	4.5V	4.5V	Q_C at t_{n+1}
D	4.5V	4.5V	Q_D at t_{n+1}
L Serial Input	4.5V	0V	Q_A at t_{n+4}
R Serial Input	0V	4.5V	Q_D at t_{n+4}



VOLTAGE WAVEFORMS

Note: A. The clock pulse generator has the following characteristics: $Z_{out} \approx 500\Omega$ and PRR≤1MHz, tr≤15ns and tf≤6ns
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or 1N916
D. A clear pulse is applied prior to each test.
E. V_{ref} = 1.3V
F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}.
Proper shifting of data is verified at t_{n+4} with a function test
G. t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transition.

Figure 1. Switching Times

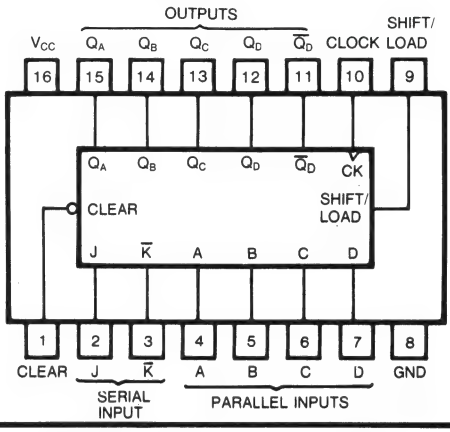
GD54/74LS195A

4-BIT PARALLEL ACCESS SHIFT REGISTERS

Features

- Synchronous parallel load
- Positive-edge-triggered clocking
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- For use in high-performance:
  accumulators/processors
  serial-to-parallel, parallel-to-serial converters
- Typical clock frequecy 39 MHz
- Typical power dissipation 70mW

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

General Description

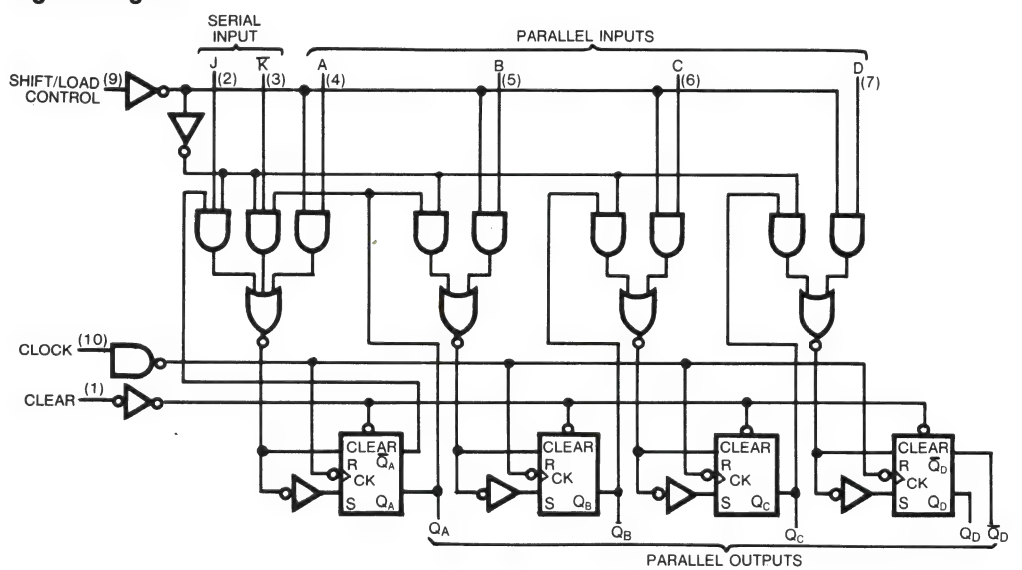
These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D, or T-type flip-flop as shown in the function table.

Logic Diagram



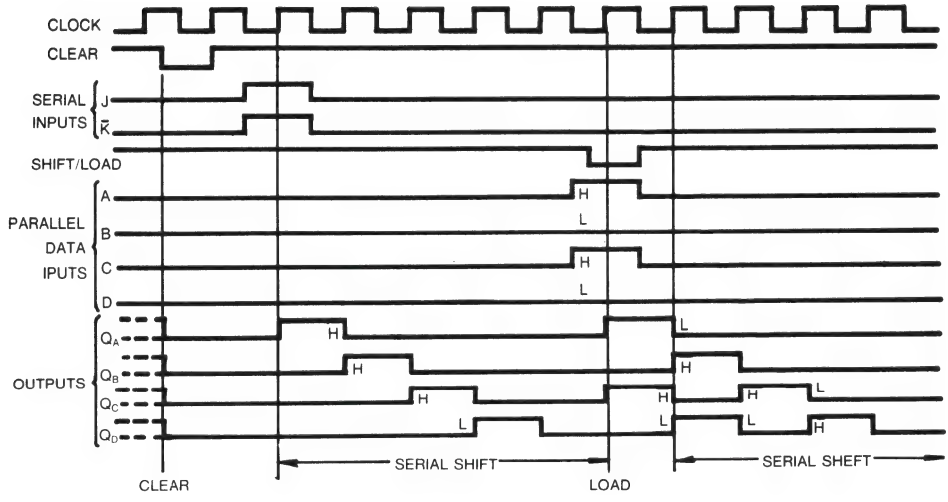
Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	d
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H=High Level (steady state), L=Low Level (steady state), X=Don't Care (any input, including transitions)
↑=Transition from low to high level
a,b,c,d=The level of steady state input at A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}=The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}= The level of Q_A, Q_B, Q_C, respectively, before the most recent transition of the clock.

Timing Diagram

TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54, 74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
f_{clock}	Clock frequency		0		30	MHz
t_w	Pulse Width	Clock	16			ns
		Clear	12			
t_{su}	Setup Time	Shift/Load	25			ns
		Data	15			
t_H	Hold Time		0			ns
t_{REL}	Shift/Load Release Time		10			ns
	Clear Release Time		25			
T_A	Operatig free-air teperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input curret at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				14	21	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
Note3: With all outputs open, SHIFT/LOAD grounded, and 4.5V applied to the J,$\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, then 4.5V to the CLEAR and then applying a momentary ground then 4.5V to the CLOCK.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency		30	39		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input	$C_L=15pF$, $R_L=2k\Omega$		19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input			14	22	ns
t_{PHL}	Propagation delay time, high-to low-level Q outputs from clock input			17	26	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS221

DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT—TRIGGER INPUTS

Feature

- Pin Out is identical to the LS123
- B input has hysterisis for improved noise immunity
- Overriding Reset terminates outpulse

Description

The LS221 contains two monostable multivibrator circuits with direct reset input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time to the input pulse A proper transition by either the CLR.A or B input, as shown in the function will cause the Q output to go high and remain high for the pulse time tw.

Output Pulse Width, t_w

The output pulse width is set using R_{ext} and C_{ext} by the following formula

$tw = C_{ext}.R_{ext}$ ln2 [ns]

$tw = 0.7 C_{ext}.R_{ext}$[ns]

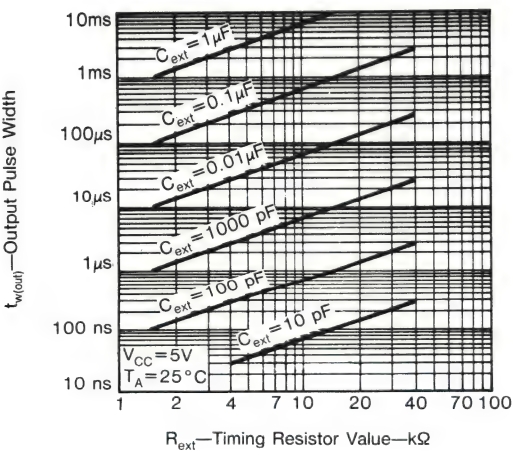
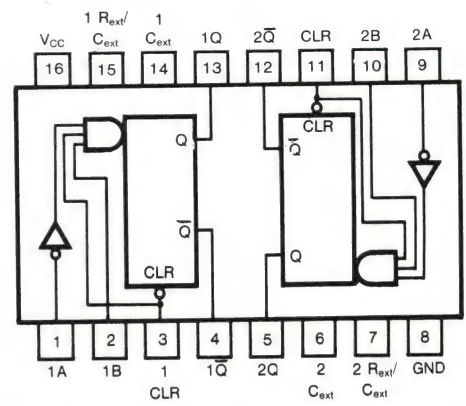


Figure 1.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

INPUT			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

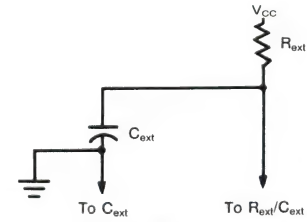


Figure 2. Connection of C_{ext} and R_{ext}

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54, 74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
dv/dt	Rate of rise or fall of input pulse	Schmitt. B		1			v/s
		Logic Input. A		1			v/μs
t_W	Input pulse width	A or B		50			ns
		Clear		40			
t_{SU}	Clear-inactive-state setup time			15			ns
R_{ext}	External timing resistance			1.4		100	kΩ
C_{ext}	External capacitance			0.		1000	μF
O.D.C	Output duty cycle		R_T=2kΩ			50	%
			R_T=Max R_{ext}			90	
T_A	Operating Free-air Temp.		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise note)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	Typ (Note 1)	MAX	UNIT
V_{T+}	Positive-Going Input Threshold Voltage at A input		V_{CC}=Min				1.0	2.0	V
V_{T-}	Negative-Going Input Threshold Voltage at A input		V_{CC}=Min			0.8	1.0		V
V_{T+}	Positive-Going Input Threshold Voltage at B input		V_{CC}=Min				1.0	2.0	V
V_{T-}	Negative-Going Input Threshold Voltage at B input		V_{CC}=Min			0.8	0.9		V
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage		V_{CC}=Min, I_{OH}=Max,	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
					74	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
				I_{OL}=8mA	74		0.35	0.5	
I_I	Input Current at Maximum Input Voltage		V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level Input Current	Input A	V_{CC}=Max, V_I=0.4V					−0.4	mA
		Input B						−0.8	
		Clear						−0.8	
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply Current		V_{CC}=Max		Quiescent		4.7	11	mA
					Triggered		19	27	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM(INPUT)	TO(OUTPUT)	TEST CONDITION#		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	$C_L=15pF$, $R_L=2k\Omega$	$C_{ext}=80pF$, $R_{ext}=2k\Omega$		48	70	ns
	B					35	55	
t_{PHL}	A	$\overline{Q}$				50	80	ns
	B					40	65	
t_{PHL}	Clear	Q	See Fig 1			35	55	ns
t_{PLH}		Q				44	65	
out	A or B	Q		$C_{ext}=80pF$, $R_{ext}=2k\Omega$	70	120	150	ns
t_wQ(out)	A or B	Q		$C_{ext}=0$, $R_{ext}=2k\Omega$	20	47	70	
				$C_{ext}=100pF$, $R_{ext}=10k\Omega$	670	740	810	
				$C_{ext}=1\mu F$, $R_{ext}=10k\Omega$	6	6.9	7.5	ms

* t_{PLH}=propagation delay time, low-to-high-level output.
* t_{PHL}=propagation delay time, high-to-low-level output.
* t_wQ=width of pulse at output Q

#For load circuit and voltage waveforms, see page 3-11.

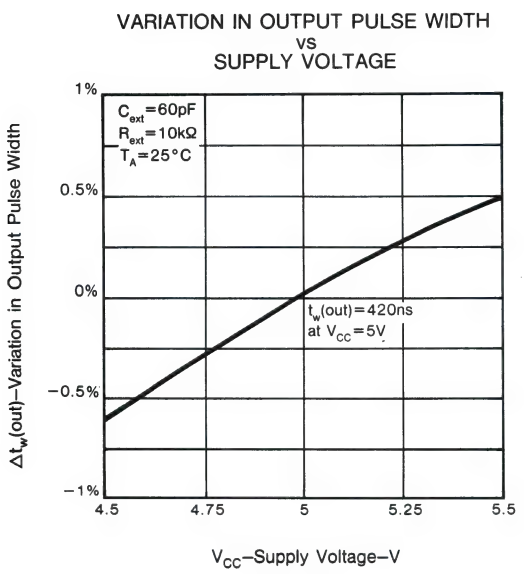


FIGURE 3

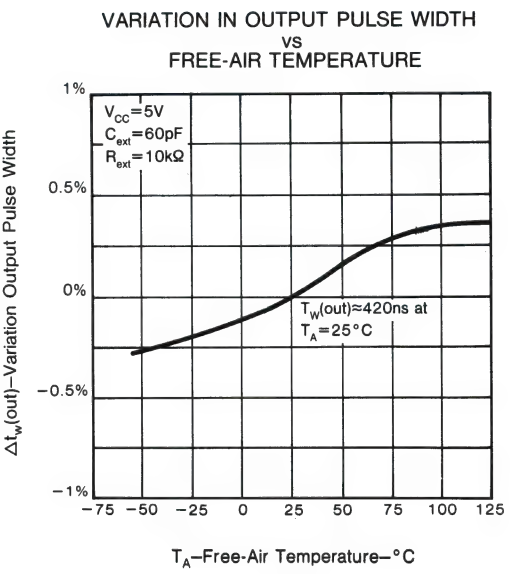
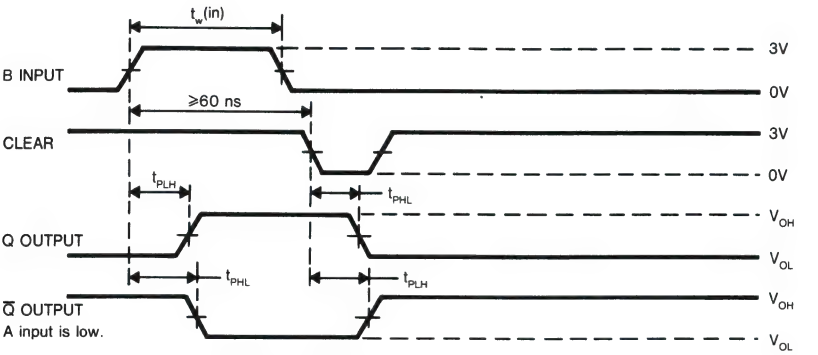
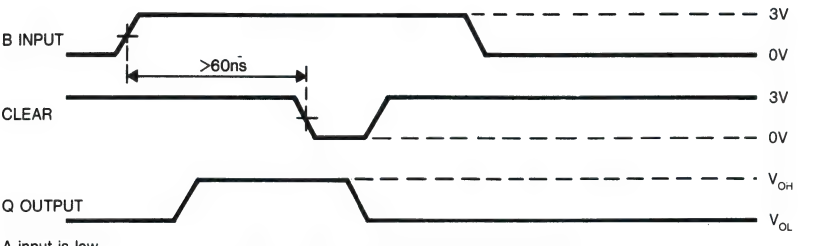


FIGURE 4

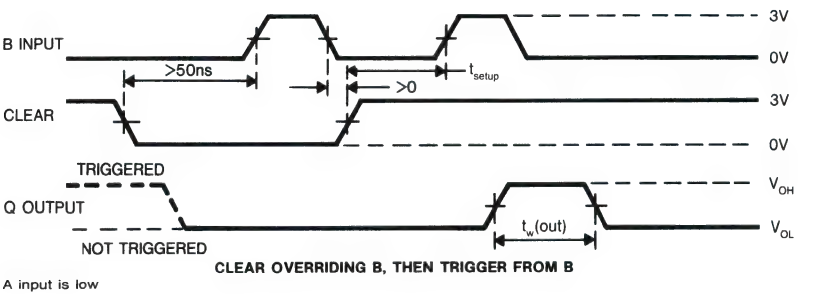
PARAMETER MEASUREMENT INFORMATION



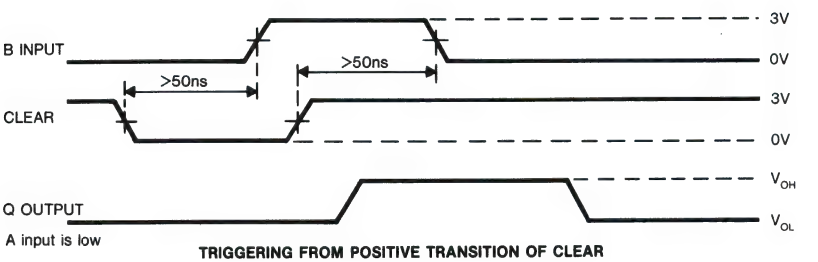
TRIGGER FROM B, THEN CLEAR-CONDITION 1



TRIGGER FROM B, THEN CLEAR-CONDITION 2



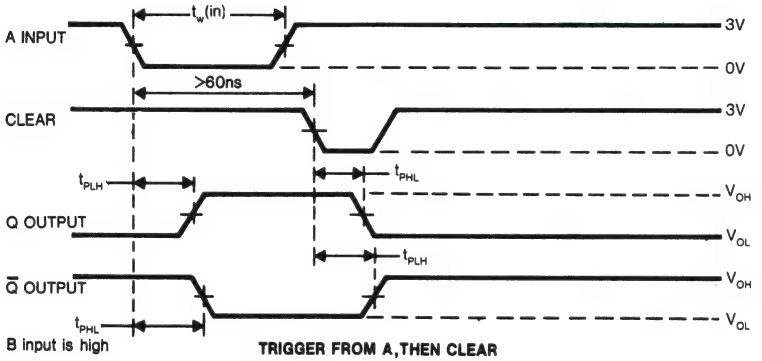
CLEAR OVERRIDING B, THEN TRIGGER FROM B



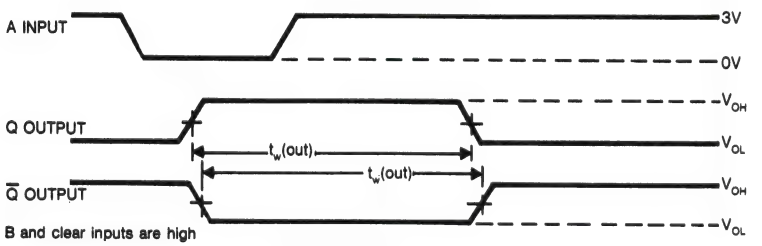
TRIGGERING FROM POSITIVE TRANSITION OF CLEAR

Figure 1. Switching Characteristics

PARAMETER MEASUREMENT INFORMATION



TRIGGER FROM A, THEN CLEAR



TRIGGER FROM A

NOTES: A. Input pulses are supplied by ganerators having the following characteristics: PRR<1 MHz, Z_{out}~50Ω: for 221, t_r<7 ns, t_f<7 ns, for LS221, t_r<15 ns, t_f<6 ns.

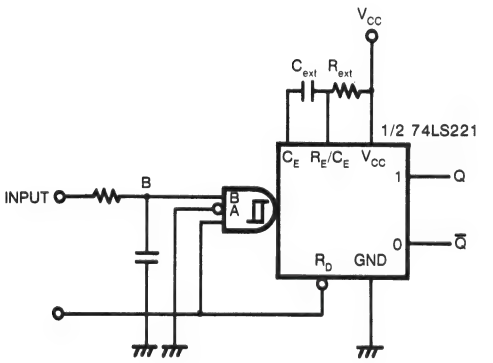
B. All measurements are made between the 1.5 V points of the indicated transitions for the 221 or between the 1.3V points for the LS221.

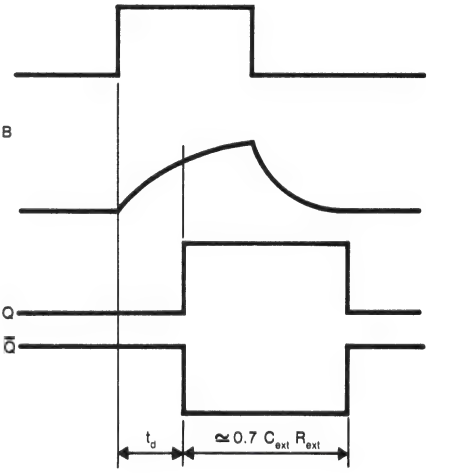
Figure 1 Switching Characteristics

Application Examples

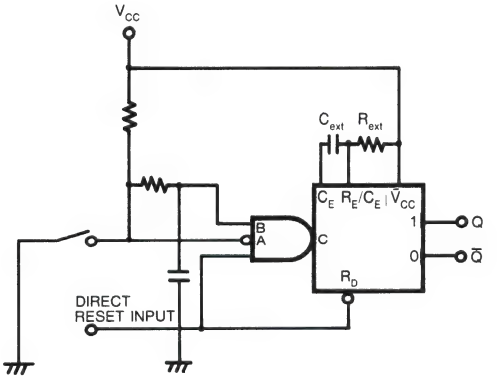
(1) Delay circut

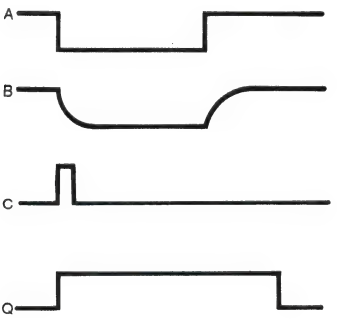
By connecting an integration circuit to the B input, a rectangular waveform applied to the input is changed to the waveform shown at B and delayed by time t_d. The width of the pulse output at Q and Q is determined as usual by the values of C_{ext}, R_{ext} connected externally to the circuit.





(2) ANTI-CHATTERING CIRCUIT





GD54/74LS240

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS INVERTED 3-STATE OUTPUTS

Feature

- 3-State outputs Drive Bus Lines or Buffer Memory Addres Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins

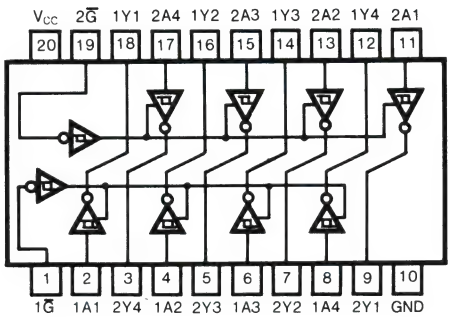
Description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

This device features high fan-out, improved fan-in and 400mV noise margin.

It can be used to drive terminated lines down to 133 ohms

Pin Configuration



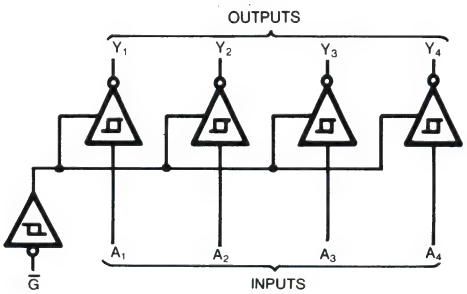
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Note: All devices have input hysteresis.

Function Block Diagram (each block)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−12	mA
		74			−15	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage				54			0.7	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA					−1.5	V
$V_{T+}-V_{T-}$	Hysteresis		V_{CC}=Min,			0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC}=Min, V_{IH}=Min V_{IL}=Max, I_{OH}=−1mA		74	2.7			V
			V_{CC}=Min, V_{IH}=Min V_{IL}=Max, I_{OH}=−3mA		54,74	2.4	3.4		
			V_{CC}=Min, V_{IH}=Min V_{IL}=0.5V, I_{OH}=Max		54,74	2			
V_{OL}	Low-level output voltage		V_{CC}=Min V_{IL}=Max V_{IH}=Min	I_{OL}=12mA	54, 74		0.25	0.4	V
				I_{OL}=24mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied		V_{CC}=Max, V_O=2.7V V_{IH}=Min, V_{IL}=Max					20	μA
I_{OZL}	Off-state output current low-level voltage applied		V_{CC}=Max, V_O=0.4V V_{IH}=Min, V_{IL}=Max					−20	μA
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.4V					−0.2	mA
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	Outputs high	V_{CC}=5.25V Outputs open				17	27	mA
		Outputs low					26	44	
		All outputs disabled					29	50	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L=45pF$, $R_L=667\Omega$		9	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	18	ns
t_{PZL}	Output enable time to low level			20	30	ns
t_{PZH}	Output enable time to high level			15	23	ns
t_{PLZ}	Output disable time from low level	$C_L=5pF$, $R_L=667\Omega$		15	25	ns
t_{PHZ}	Output disable time from high level			10	18	ns

For load circuit and voltage waveforms, see page 3-11.

GD54/74LS241

OCTAL BUFFER/LINE DRIVERS/ LINE RECEIVERS NON INVERTED 3-STATE OUTPUTS OUTPUTS

Feature

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins

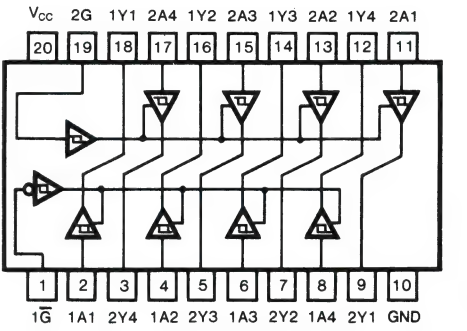
Description

These octal buffers and line drivers are desinged specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and busoriented receivers and transmitters.

This device features high fan-out, improved fan-in, and 400mV noise margin.

It can be used to drive terminated lines down to 133 ohms

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

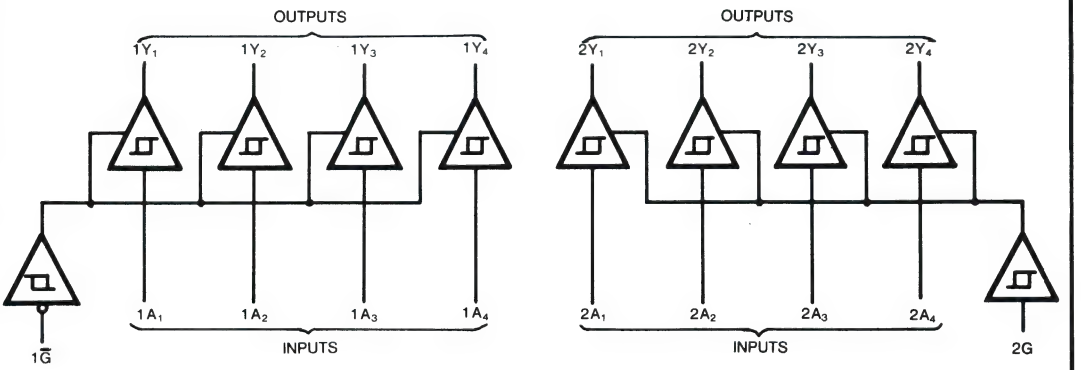
Function Table (Note 1)

1A	1 $\bar{G}$	1Y
L	L	L
H	L	H
X	H	Z

2A	2 G	2Y
L	H	L
H	H	H
X	L	Z

Note 1 Z: High-impedance
X: irrelevant

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−12	mA
		74			−15	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC}=Min,			0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IH}=Min V_{IL}=Max, I_{OH}=−1mA		74	2.7			V
		V_{CC}=Min, V_{IH}=Min V_{IL}=Max, I_{OH}=−3mA		54,74	2.4	3.4		
		V_{CC}=Min, V_{IH}=Min V_{IL}=0.5V, I_{OH}=Max		54,74	2			
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max V_{IH}=Min	I_{OL}=12mA	54, 74		0.25	0.4	V
			I_{OL}=24mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.7V V_{IH}=Min, V_{IL}=Max					20	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.4V V_{IH}=Min, V_{IL}=Max					−20	μA
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	Outputs high	V_{CC}=5.25V, Outputs open			17	27	mA
		Outputs low				26	46	
		All outputs disabled				32	54	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L=45pF$, $R_L=667\Omega$		12	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	18	ns
t_{PZL}	Output enable time to low level			20	30	ns
t_{PZH}	Output enable time to high level			15	23	ns
t_{PLZ}	Output disable time from low level	$C_L=5pF$, $R_L=667\Omega$		15	25	ns
t_{PHZ}	Output disable time from high level			10	18	ns

For load circuit and voltage waveforms, see page 3-11.

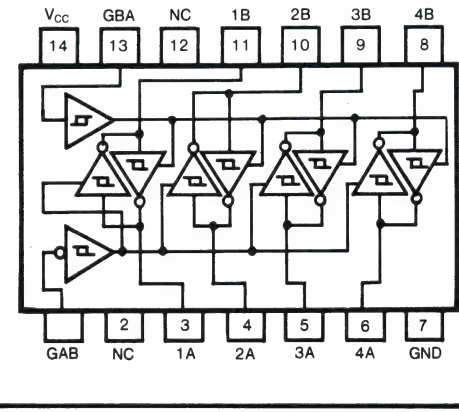
GD54/74LS242

QUADRUPLE BUS TRANSCEIVERS

Features

- Two-Way Asynchronous Communication Between Data Buses
- P-N-P Inputs Reduce D-C Loading
- Hysteresis (Typically 400 mV) at Inputs Improves Noise Margin
- High Fan out (I_{OL}=24mA)

Pin Configuration

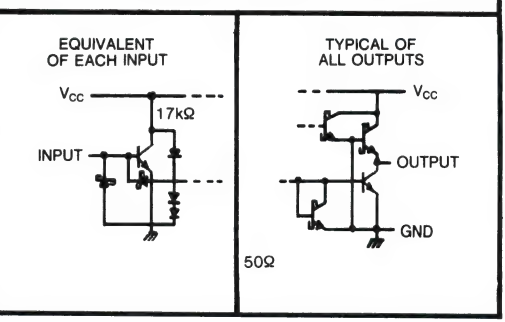


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

These four data line transceivers are designed for asynchronous two-way communications between data buses. They can be used to drive terminated lines down to 133 ohms.

schematics of inputs and outputs



Function Table

CONTROL INPUTS		'LS242 DATA PORT STATUS	
$\overline{G}$AB	GBA	A	B
H	H	$\overline{O}$	I
L	H	*	*
H	L	ISOLATED	
L	L	I	$\overline{O}$

*Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.
I=input, O=Output, $\overline{O}$=Inverting Output.

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage Any G 7V
  A or B 5.5V
- Operating free-air temperature range ..... 0°C to 70°C
  ..... −55°C to 25°C
- Storage teperature rage ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−12	mA
		74			−15	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC}=Min			0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IH}=Min, V_{IL}=Max, I_{OH}=−1mA		74	2.7			V
		V_{CC}=Min, V_{IH}=Min, V_{IL}=Max, I_{OH}=−3mA		54, 74	2.4	3.4		
		V_{CC}=Min, V_{IH}=Min, V_{IL}=0.5V, I_{OH}=Max		54, 74	2			
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=12mA	54, 74		0.25	0.4	V
			I_{OL}=Max	74		0.35	0.5	
I_{OZH}	Off-state output curret high-level voltage applied	V_{CC}=Max, V_O=2.7V, V_{IH}=Min, V_{IL}=Max,					40	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.4V, V_{IH}=Min, V_{IL}=Max					−200	μA
I_I	Input current at maximun input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	Output high	V_{CC}=5.25V Outputs open			22	38	mA
		Outputs low				29	50	
		All outputs disabled				29	50	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAETER	TEST CONDITION	'LS242			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L=45pF$, $R_L=667\Omega$,		9	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	18	ns
t_{PZL}	Output enable time to low level			20	30	ns
t_{PZH}	Output enable time to high level			15	23	ns
t_{PLZ}	Output disable time from low level	$C_L=5pF$, $R_L=667\Omega$,		15	25	ns
t_{PHZ}	Output disable time from high level			10	18	ns

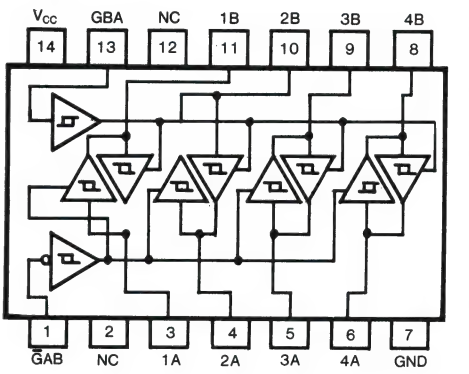
#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS243
QUADRUPLE BUS TRANSCEIVERS

Features

- Two-Way Asynchronous Communication Between Data Buses
- P-N-P Inputs Reduce D-C Loading
- Hysteresis (Typically 400 mV) at Inputs Improves Noise Margin
- High Fan out (I_{OL}=24mA)

Pin Configuration

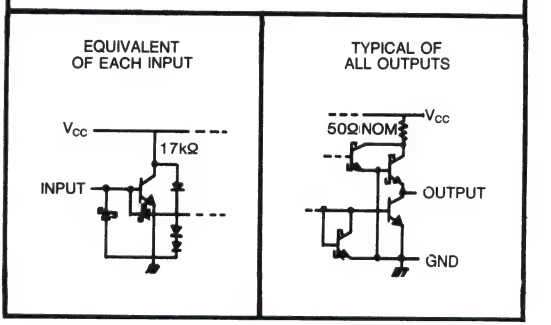


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

These four data line transceivers are designed for asynchronous two-way communications between data buses. They can be used to drive terminated lines down to 133 ohms.

Schematics of Inputs and Outputs



Function Table

CONTROL INPUTS		'LS243 DATA PORT STATUS	
$\overline{G}$AB	GBA	A	B
H	H	O	I
L	H	*	*
H	L	ISOLATED	
L	L	I	O

*Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.
I=input, O=Output.

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage Any G 7V
  A or B 5.5V
- Operating free-air temperature range ..... 0°C to 70°C
  ..... −55°C to 25°C
- Storage teperature rage ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−12	mA
		74			−15	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC}=Min			0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IH}=Min, V_{IL}=Max, I_{OH}=−1mA		74	2.7			V
		V_{CC}=Min, V_{IH}=Min, V_{IL}=Max, I_{OH}=−3mA		54, 74	2.4	3.4		
		V_{CC}=Min, V_{IH}=Min, V_{IL}=0.5V, I_{OH}=Max		54, 74	2			
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=12mA	54, 74		0.25	0.4	V
			I_{OL}=Max	74		0.35	0.5	
I_{OZH}	Off-state output curret high-level voltage applied	V_{CC}=Max, V_O=2.7V, V_{IH}=Min, V_{IL}=Max					40	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.4V, V_{IH}=Min, V_{IL}=Max					−200	μA
I_I	Input current at maximun input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	Outputs high	V_{CC}=5.25V, Outputs open			22	38	mA
		Outputs low				29	50	
		All outputs disabled				32	54	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAETER	TEST CONDITION #	LS243			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L=45pF$, $R_L=667\Omega$,		12	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	18	ns
t_{PZL}	Output enable time to low level			20	30	ns
t_{PZH}	Output enable time to high level			15	23	ns
t_{PLZ}	Output disable time from low level	$C_L=5pF$, $R_L=667\Omega$,		15	25	ns
t_{PHZ}	Output disable time from high level			10	18	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS244

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS NONINVERTED 3-STATE OUTPUTS

Feature

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins

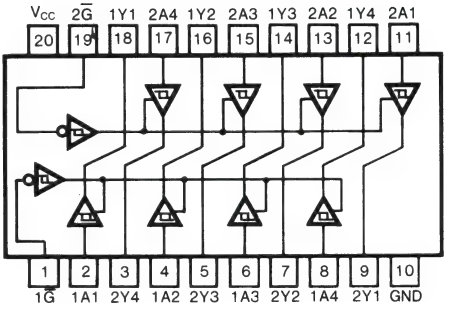
Description

These octal buffers and line drivers and designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and busoriented receivers and transmitters.

This device features high fan-out, improved fan-in, and 400mV noise margin.

It can be used to drive terminated lines down to 133 ohms

Pin Configuration



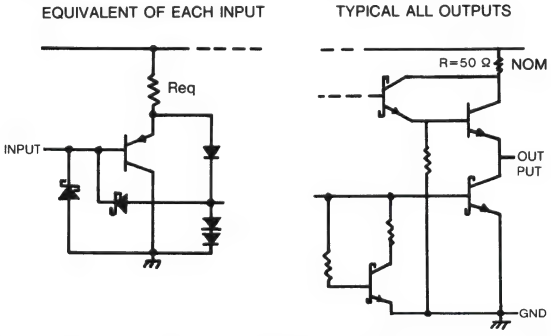
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

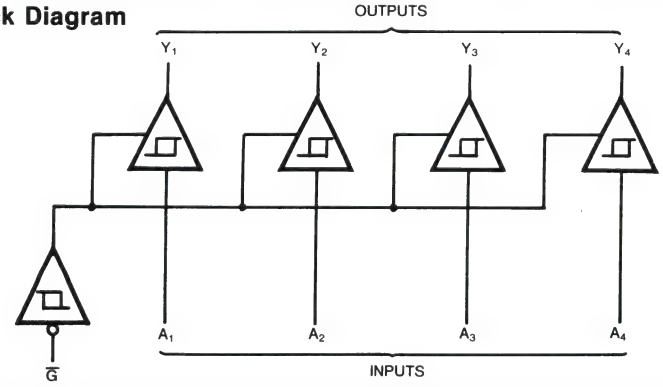
A	$\overline{G}$	Y
L	L	L
H	L	H
X	H	Z

X: Irrelevant
Z: High Impedance

Schematics of Inputs and Outputs



Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−12	mA
		74			−15	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC}=Min			0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IH}=Min, V_{IL}=Max, I_{OH}=−1mA		74	2.7			V
		V_{CC}=Min, V_{IH}=Min, V_{IL}=Max, I_{OH}=−3mA		54,74	2.4	3.4		
		V_{CC}=Min, V_{IH}=Min, V_{IL}=0.5V, I_{OH}=Max		54,74	2			
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=12mA	54, 74		0.25	0.4	V
			I_{OL}=24mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.7V, V_{IH}=Min, V_{IL}=Max					20	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.4V, V_{IH}=Min, V_{IL}=Max					−20	μA
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	Outputs high	V_{CC}=5.25V Outputs open			17	27	mA
		Outputs low				27	46	
		All outputs disabled				32	54	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L=45pF$, $R_L=667\Omega$		12	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	18	ns
t_{PZL}	Output enable time to low level			20	30	ns
t_{PZH}	Output enable time to high level			15	23	ns
t_{PLZ}	Output disable time from low level	$C_L=5pF$, $R_L=667\Omega$		15	25	ns
t_{PHZ}	Output disable time from high level			10	18	ns

For load circuit and voltage waveforms, see page 3-11.

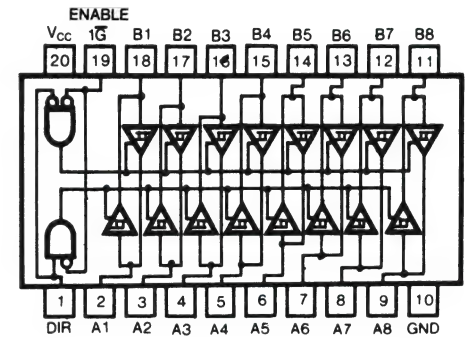
GD54/74LS245

OCTAL BUS TRANSCEIVER; NON-INVERTED 3-STATE OUTPUTS

Feature

- Bidirectional Bus Transceiver in a High-Density 20-Pin Package
- 3-State Outputs Dirve Bus Lines Directly
- P-N-P Inputs D-C Loading on Bus Lines
- Hysteresis at Bus Inputs Improve Noise Margins
- Typical Propagation Delay Times; Port to Port ... 8 ns

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

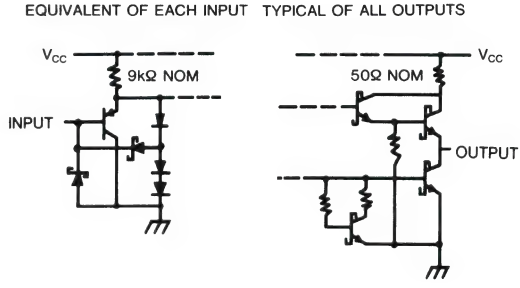
These octal bus transceiver are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the directional control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

Function Table

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Schematics of Inputs and Outputs



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Off-state output voltage 5.5V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−12	mA
		74			−15	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage				54			0.7	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA					−1.5	V
$V_{T+}-V_{T-}$	Hysteresis		V_{CC}=Min,			0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC}=Min, V_{IH}=Min V_{IL}=Max, I_{OH}=−1mA		74	2.7			V
			V_{CC}=Min, V_{IH}=Min V_{IL}=Max, I_{OH}=−3mA		54,74	2.4	3.4		
			V_{CC}=Min, V_{IH}=Min V_{IL}=0.5V, I_{OH}=Max		54,74	2			
V_{OL}	Low-level output voltage		V_{CC}=Min V_{IL}=Max V_{IH}=Min	I_{OL}=12mA	54, 74		0.25	0.4	V
				I_{OL}=24mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied		V_{CC}=Max, V_O=2.7V V_{IH}=Min, V_{IL}=Max		$\overline{G}$ at 2V			20	μA
I_{OZL}	Off-state output current low-level voltage applied		V_{CC}=Max, V_O=0.4V V_{IH}=Min, V_{IL}=Max		$\overline{G}$ at 2V			−200	μA
I_I	Input current at maximum maximum input voltage	A or B	V_{CC}=Max		V_I=5.5V			0.1	mA
		DIR or $\overline{G}$			V_I=7V				
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.4V					−0.2	mA
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	Outputs high	V_{CC}=5.25V, Outputs open				48	70	mA
		Outputs low					62	90	
		All outputs disabled					64	95	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L=45pF$, $R_L=667\Omega$		8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output			8	12	ns
t_{PZL}	Output enable time to low level			27	40	ns
t_{PZH}	Output enable time to high level			25	40	ns
t_{PLZ}	Output disable time from low level	$C_L=5pF$, $R_L=667\Omega$		15	25	ns
t_{PHZ}	Output disable time from high level			15	25	ns

For load circuit and voltage waveforms, see page 3-11.

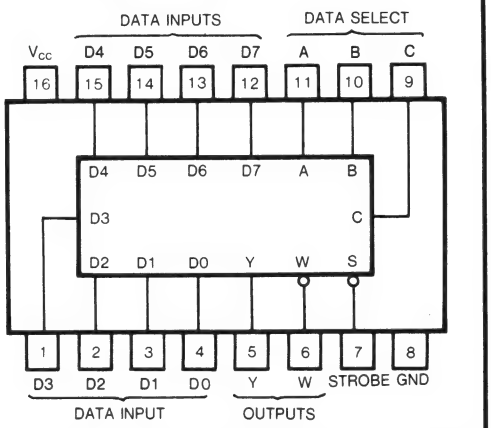
GD54/74LS251

8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUT

Features

- 3-State Versions of LS151
- Three-State Outputs Interface Directly with System Bus
- Performs Parallel-to-Serial Conversion
- Complementy Outputs Provide True and Inverted Data
- Fully Compatible with Most TTL Circuits

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : .Ceramic Dual In Line Package

Description

These monorithic data selectors/multiplexers contain full on chip binary decoding to select one-of-eight data sources and feature a strobe controlled three state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit a numer of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high impedance state in which both the upper and lower transistors of each totem-pole output are off and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem pole outputs.

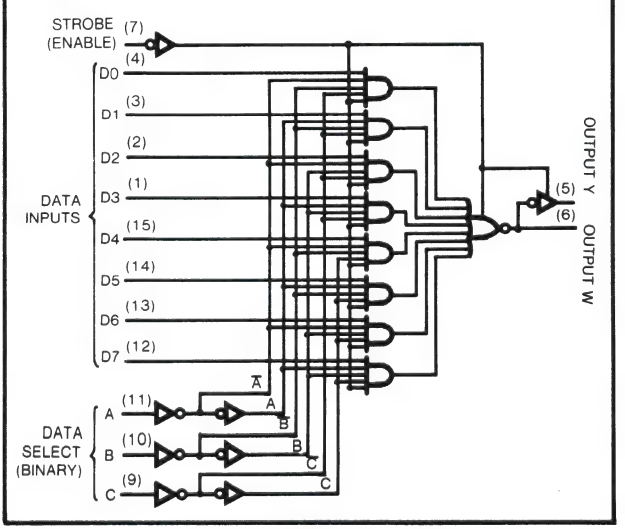
GD54/74LS 251 has the same functions and pin connections as GD54/74LS151 but the latter is provided with active pull-up resistors outputs.

Function Table

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H=high logic level. L=low logic level
X=irrelevant. Z=high impedance (off)
D0.D1...D7=the level of the respective D input

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Off-state output voltae 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	4	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−1	mA
		74			−2.6	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max I_{OH}=Max, V_{IH}=Min		54	2.4	3.4		V
				74	2.4	3.1		
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max V_{IH}=Min	I_{OL}=12mA	54,74		0.25	0.4	V
			I_{OL}=24mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.7V. V_{IH}=Min, V_{IL}=Max					20	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.4V V_{IH}=Min, V_{IL}=Max					−20	μA
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)	Condition A			6.1	10	mA
			Condition B			7.1	12	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: Condition A: I_{CC} is measured with the outputs open, strobe grounded, and all other inputs at 4.5V.
Condition B: I_{CC} is measured with the outputs open, and all inputs at 4.5V

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	A,B or C(4 levels)	Y	$C_L=15pF$ $R_L=2k\Omega$		29	45	ns
t_{PHL}					28	45	
t_{PLH}	A,B, or C (3 levels)	W			20	33	ns
t_{PHL}					21	33	
t_{PLH}	Any D	Y			17	28	ns
t_{PHL}					18	28	
t_{PLH}	Any D	W			10	15	ns
t_{PHL}					9	15	
t_{PZH}	Strobe	Y			30	45	ns
t_{PZL}					26	40	
t_{PZH}	Strobe	W			17	27	ns
t_{PZL}					24	40	
t_{PHZ}	Strobe	Y	$C_L=5pF$ $R_L=2k\Omega$		30	45	ns
t_{PLZ}					15	25	
t_{PHZ}	Strobe	W			37	55	ns
t_{PLZ}					15	25	

* t_{PLH}=propagation delay time, low-to-high-level output
* t_{PHL}=propagation delay time, high-to-low-level output
* t_{PZH}=output enable time to high level
* t_{PZL}=output enable time to low level
* t_{PHZ}=output disable time from high level
* t_{PLZ}=output disable time from low level

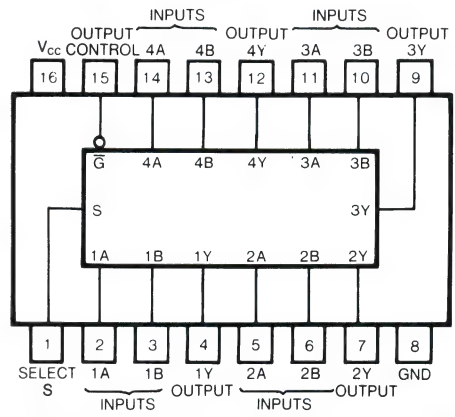
#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS257A
QUAD DATA SELECTORS/MULTIPLEXERS; NON-INVERTED 3-STATE OUTPUTS

Feature

- Three-State Outputs Interface Directly with System Bus
- Provides Bus Interface from Multiple Sources in High-Performance System
- 3-State Versions LS157 with Same Pin Outs

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

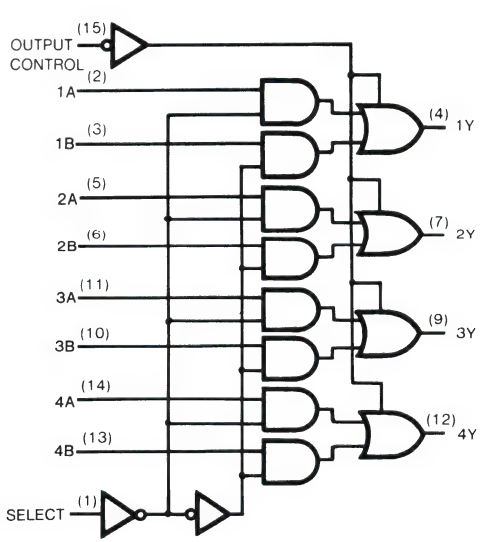
Description

This device is designed to multiplex singals from four bit data sources to four-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin ($\overline{G}$) is at high-logic level.

Funciton Table

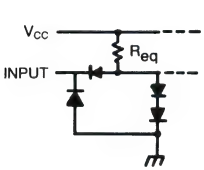
INPUTS				OUTPUT
OUTPUT CONTROL	SELECT	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Function Block Diagram

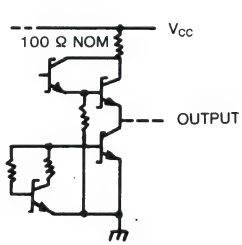


Schematics of Inputs and Outputs

TYPICAL OF ALL OUTPUTS



EQUIVALENT OF EACH INPUT



Select. R_{eq}=9.5 kΩ NOM
All other inputs. R_{eq}=19 kΩ NOM

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Off-state output voltage 5.5V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−1	mA
		74			−2.6	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min		54	2.4	3.4		V
				74	2.4	3.1		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=12mA	54 74		0.25	0.4	V
			I_{OL}=24mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.7V, V_{IH}=Min, V_{IL}=Max					20	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.4V, V_{IH}=Min, V_{IL}=Max					−20	μA
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	S input				0.2	mA
			Any other				0.1	
I_{IH}	High-level Input current	V_{CC}=Max, V_I=2.7V	S input				40	μA
			Any other				20	
I_{IL}	Low-level Input current	V_{CC}=Max, V_I=0.4V	S input				−0.8	mA
			Any other				−0.4	
I_{OS}	Short circuit output current	V_{CC}=Max			−20		−100	mA
I_{CC}	Supply Current	All outputs high	V_{CC}=5.25V, (Note 3)			6.2	10	mA
		All outputs low				10	16	
		All outputs off				12	19	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

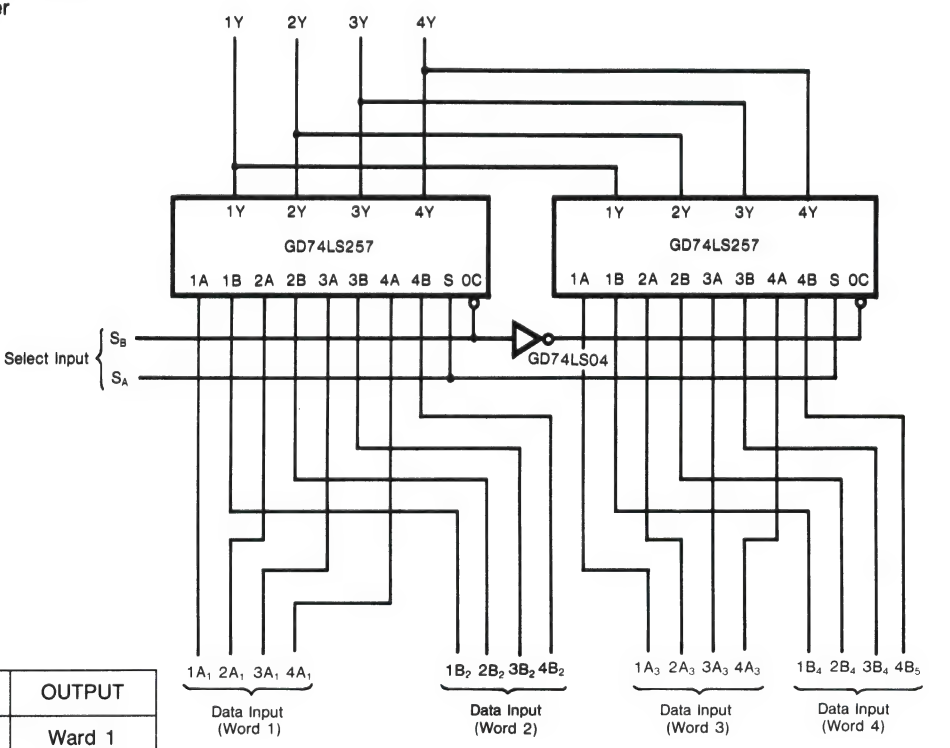
PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Any	$C_L=45pF$		8	18	ns
t_{PHL}					13	18	
t_{PLH}	Select	Any			18	28	ns
t_{PHL}					22	35	
t_{PZH}	Output Control	Any			14	22	ns
t_{PZL}					22	35	
t_{PHZ}	Output Control	Any	$C_L=5pF$		16	26	ns
t_{PLZ}					22	35	

* t_{PLH}=propagation delay time, low-to-high-level output, t_{PZL}=output enable time to low level
* t_{PHL}=propagation delay time, high-to-low-level output, t_{PHZ}=output disable time from high level.
* t_{PZH}=output enable time to high level, t_{PLZ}=output disable time from low level.

#For load circuit and voltage waveforms, see page 3-11.

Application Example

8-Bit shift register



S_A	S_B	OUTPUT
L	L	Ward 1
L	H	Word 2
H	L	Word 3
H	H	Word 4

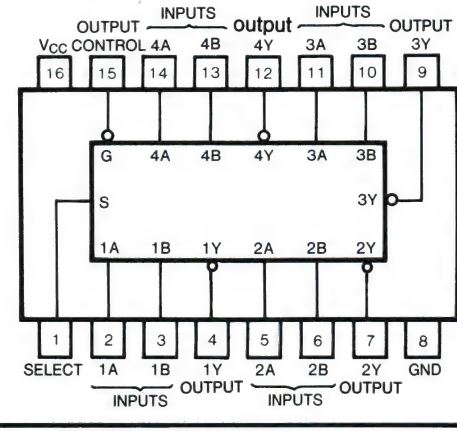
GD54/74LS258B

QUAD DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS (INVERTED)

Features

- TRI-STATE versions LS158 with same pin-outs
- Schottky-clamped for significant improvement in A-C performance
- Inverted outputs
- Output control input common to all four circuits
- Select input common to all four circuits
- 3-state outputs

Pin Configuration

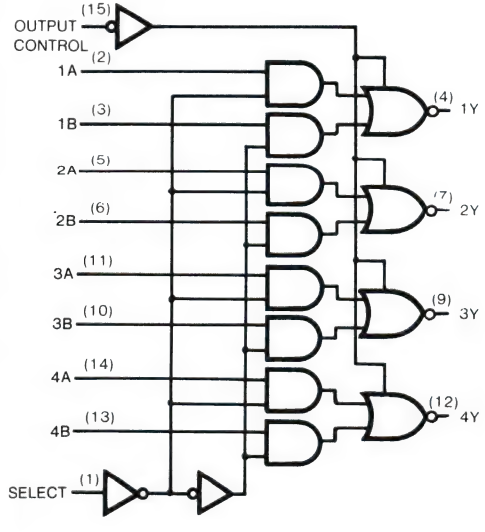


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

These Schottky-clamped high-performance multiplexers feature TRI-STATE outputs that can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times.
This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

Function Block Diagram



Function Table

INPUTS			OUTPUT
OUTPUT CONTROL	SELECT	A B	Y
H	X	X X	Z
L	L	L X	H
L	L	H X	L
L	H	X L	H
L	H	X H	L

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−1	mA
		74			−2.6	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.4	3.4		V
		I_{OH}=Max, V_{IH}=Min		74	2.4	3.1		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=12mA	54,74		0.25	0.4	V
			I_{OL}=24mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.7V, V_{IH}=Min, V_{IL}=Max					20	μA
I_{OZL}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=0.4V, V_{IH}=Min, V_{IL}=Max					−20	μA
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	S input				0.2	mA
			Any other				0.1	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	S input				40	μA
			Any other				20	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	S input				−0.8	mA
			Any other				−0.4	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply Current, Outputs high	V_{CC}=5.25V, See Note 3				4.5	7	mA
	Supply Current, Outputs low					8.8	14	
	Supply Current, All outputs disabled					12	19	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with all output open and all possible inputs grounded while achieving the stated output conditions.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Any	$C_L=45pF$ $R_L=667\Omega$		8	18	ns
t_{PHL}					13	18	
t_{PLH}	Select	Any			18	28	ns
t_{PHL}					22	35	
t_{PZH}	Output Control	Any			14	22	ns
t_{PZL}					22	35	
t_{PHZ}	Output Control	Any	$C_L=5pF$ $R_L=667\Omega$		16	26	ns
t_{PLZ}					22	35	

* t_{PLH}=propagation delay time, low-to-high-level output, t_{PZL}=output enable time to low level
* t_{PHL}=propagation delay time, high-to-low-level output, t_{PHZ}=output disable time from high level.
* t_{PZH}=output enable time to high level, t_{PLZ}=output disable time from low level.

#For load circuit and voltage waveforms, see page 3-11.

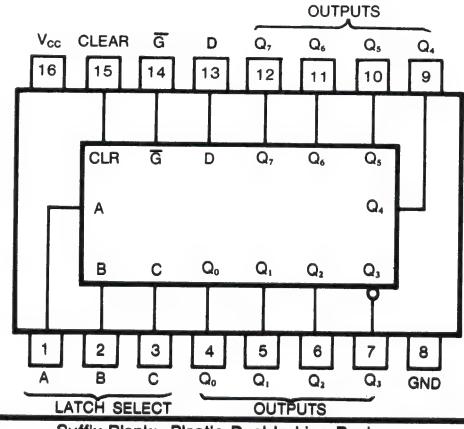
GD54/74LS259

8-BIT ADDRESSABLE LATCHES

Features

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion With Storage
- Asynchronous Parallel Clear
- Active High Decoder
- Enable/Disable Input Simplifies Expansion
- Direct Replacement for Fairchild 9334
- Expandable for N-Bit Applications
- Four Distinct Function Modes

Pin Configuration



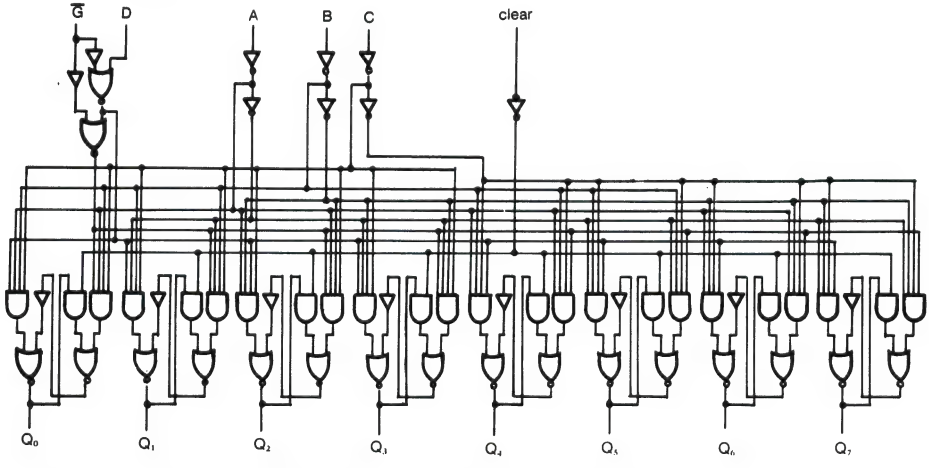
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

MODE SELECT TABLE

$\overline{G}$	$\overline{CLR}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

Function Table

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{G}$	D	A	B	C	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
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L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Memory
H	L	L	L	L	L	L	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Addressable
H	L	H	L	L	L	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Latch
H	L	L	H	L	L	Q_{t-1}	L	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	
H	L	H	H	L	L	Q_{t-1}	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	
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H	L	L	H	H	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	L	
H	L	H	H	H	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	H	

Q_{t-1}= Previous Output State X = Immaterial
H = High Voltage Level Z = High Impedance
L = Low Voltage Level

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54,74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
t_W	Pulse Width	Enable		15			ns
		Clear		15			
t_{SU}	Data setup time	Data		15↑			ns
		Select		15↓			
t_H	Data hold time	Data		0↑			ns
		Select		0↑			
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
		I_{OH}=Max, V_{IH}=Min		74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input volrage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				22	36	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with all inputs at 4.5V, and all outputs open.

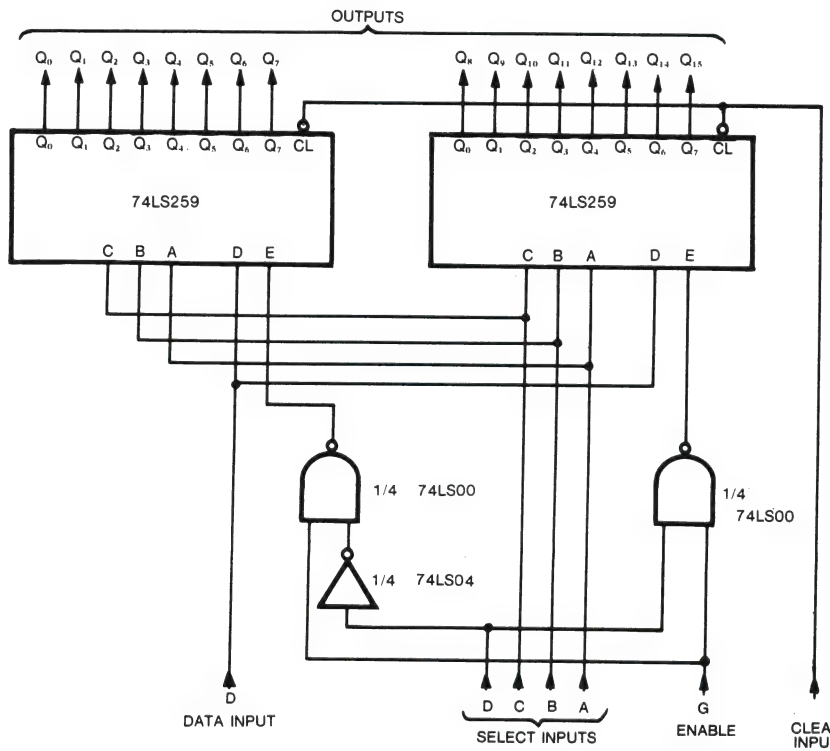
Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Enable	Output	$C_L=45pF$ $R_L=2k\Omega$		22	35	ns
t_{PHL}					15	24	
t_{PLH}	Data	Output			20	32	ns
t_{PHL}					13	21	
t_{PLH}	Select	Output			24	38	ns
t_{PHL}					18	29	
t_{PHL}	Clear	Output			17	27	

#For load circuit and voltage waveforms, see page 3-11.

Application Example

16-BIT ADDRESSABLE LATCH



GD54/74LS273

OCTAL D-TYPE FLIP-FLOPS
COMMON CLOCK SINGLE-RAIL OUTPUTS

Feature

- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

Description

These monolithic, positive edge triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

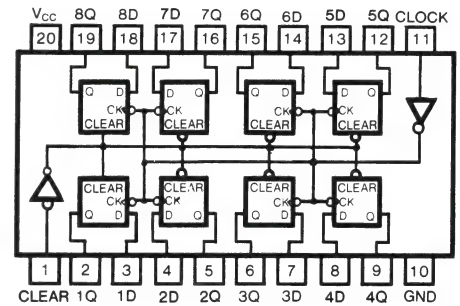
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 megahertz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 10 milliwatts.

Function Table

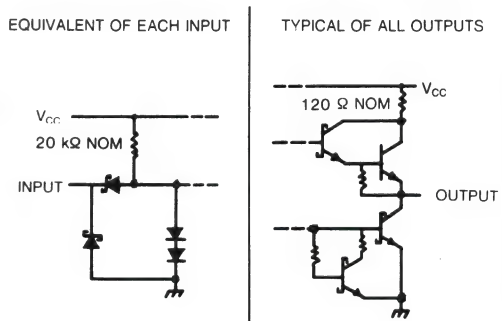
INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

Pin Configuration

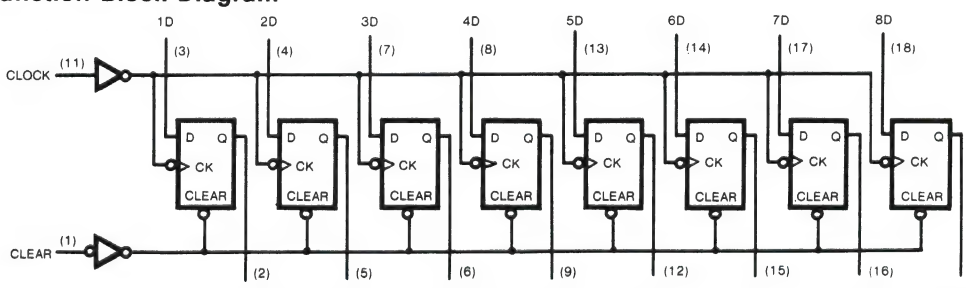


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Schematics of Inputs and Outputs



Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
f_{clock}	Clock frequency		0		30	MHz
t_w	Width of clock or clear pulse		20			ns
t_{su}	Set up time	Data input	20↑			ns
		Clear inactive-state	25↑			
t_h	Data hold time		5↑			ns
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

* ↑ The arrow indicates that the rising edge of the clock pulse is used for reference.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
		I_{OH}=Max, V_{IH}=Min		74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 3)				17	27	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
Note 3: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary grounded, then 4.5V is applied to clock.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	$C_L=15pF$, $R_L=2k\Omega$	30	40		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			17	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			18	27	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS280

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

Feature

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits
- Can Be Used to upgrade Existing Systems Using MSI Parity Circuits
- Typical Power Dissipation: 80mW

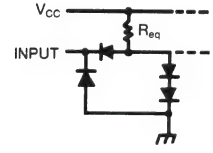
Description

These universal, monolithic, nine-bit parity generators/checkers utilize schottky-clamped TTL high performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity application. The wordlength capability is easily expanded by cascading.

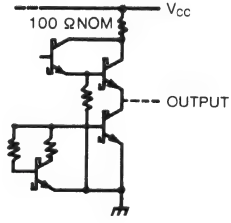
This device can be used to upgrade the performance of most systems utilizing the 180 parity generator/checker. Although the LS280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3.

Schematics of Linputs and Outputs

EQUIVALENT OF EACH INPUT

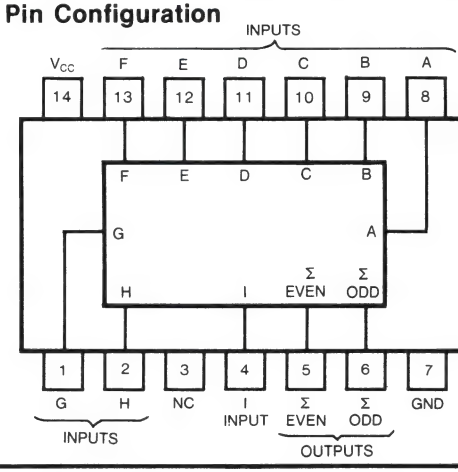


TYPICAL OF ALL OUTPUTS



Select, R_{eq}=9.5 kΩ NOM
All other inputs. R_{eq}=19 kΩ NOM

Pin Configuration

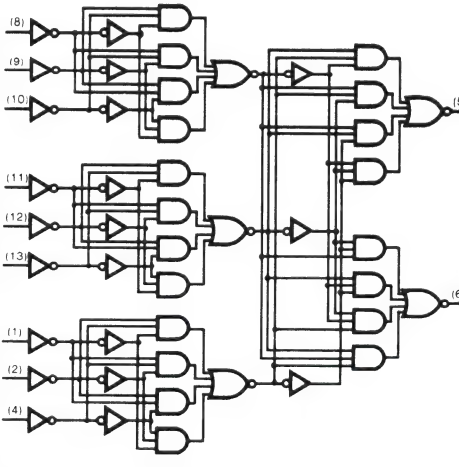


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	ΣEVEN	ΣODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
		I_{OH}=Max, V_{IH}=Min		74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V, (Note 3)				16	27	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Σ Even	C_L=15pF, R_L=2kΩ		33	50	ns
t_{PHL}					29	45	
t_{PLH}	Data	Σ Odd			23	35	ns
t_{PHL}					31	50	

t_{PLH}=propagation delay time low to high level output
t_{PHL}=propagation delay time, high to low level output
#For load circuit and voltage waveforms, see page 3-11.

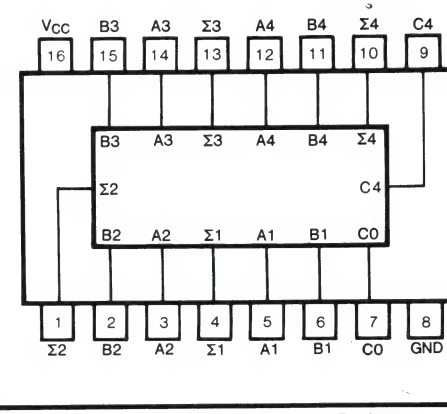
GD54/74LS283

4-BIT BINARY ADDERS WITH FAST CARRY

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
  Two 8-bit words 25 ns
  Two 16-bit words 45 ns
- Typical power dissipation per 4-bit adder 95 mW

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Descriptions

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial lookahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Function Table

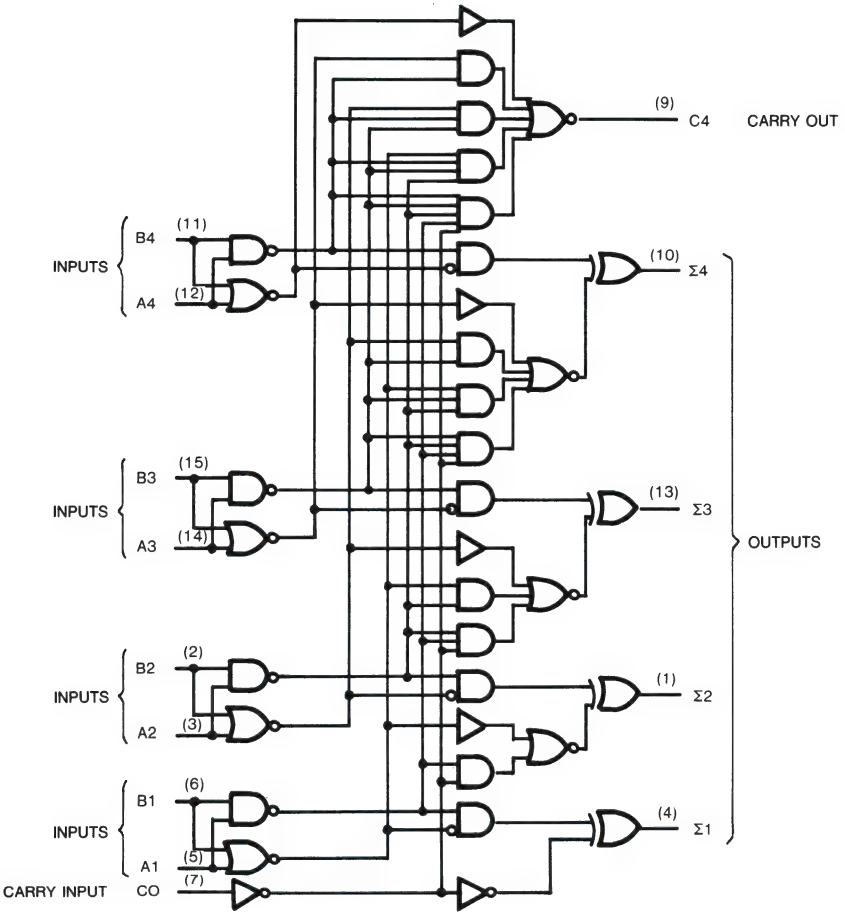
Input				Output					
				When C0=L			When C0=H		
				When C2=L			When C2=H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H=High Level, L=Low Level

Note

Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal C2. The velues at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
T_A	Operating free-air teperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−.15	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max,	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	A,B				0.2	V
			C0				0.1	
I_{IH}	High-level input current	V_{CC}=Max, V_L=2.7V	A,B				40	μA
			C0				20	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	A,B				−0.8	mA
			C0				−0.4	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max	(Note 3)	I_{CC1}		19	34	mA
			(Note 4)	I_{CC2}		22	39	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC1} is measured with all outputs open, all B input low and all other inputs at 4.5V, or all inputs at 4.5V.
Note 4: I_{CC2} is measured with all outputs open and all inputs grounded.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Σ1, Σ2, Σ3, Σ4	$C_L=15pF$, $R_L=2k\Omega$		16	24	ns
t_{PHL}					15	24	
t_{PLH}	Ai or Bi	Σi			15	24	ns
t_{PHL}					15	24	
t_{PLH}	C0	C4			11	17	ns
t_{PHL}					11	22	
t_{PLH}	Ai or Bi	C4			11	17	ns
t_{PHL}					12	17	

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS298

QUAD 2 INPUT MULTIPLEXER WITH SRORAGE

Feature

- Select From 2 Data Source
- Edge Triggered Operation

Description

The LS298 is four 2-line to 1-line multiplexers followed by a quad 4 bit edge triggered register.

When the word select input is low, data input D1(A1,B1,C1,D1) is selected, and when it is high, data input D2 (A2,B2,C2,D2) is selected.

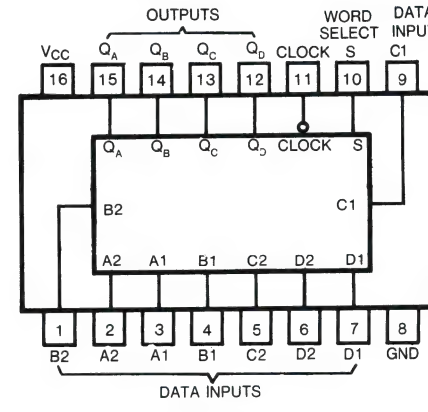
The selected data is transfered to the output Q synchronous when the clock input (CK) changes from high to low.

Function Table

INPUTS				OUTPUTS
CK	S	D_1	D_2	Q
↓	L	L	X	L
↓	L	H	X	H
↓	H	X	L	L
↓	H	X	H	H

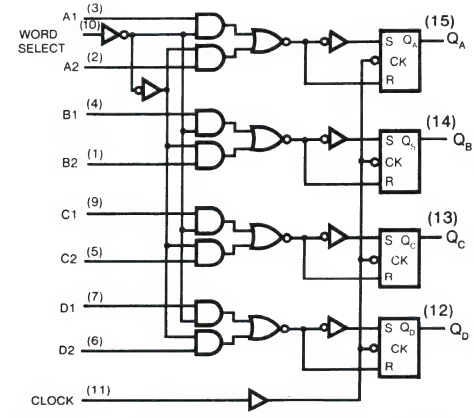
H: High level
L: Low level
X: Irrelevant
$D_1 = A_1, B_1, C_1, D_1$
$D_2 = A_2, B_2, C_2, D_2$

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Block Diagram and Logic



Dynamic input activated by a transition from a high level to a low level

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54,74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
t_{SU}	Data setup time	Data		15			ns
		Select		25			
t_H	Data hold time	Data		5			ns
		Select		0			
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	HIgh-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				13	21	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with S, A1~D_2 inputs grounded and a momentary 4.5V, then grounded, applied $\overline{CK}$ input.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PRAAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=2kΩ		18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output			21	32	ns

#For load circuit and voltage waveforms, see page 3-11.

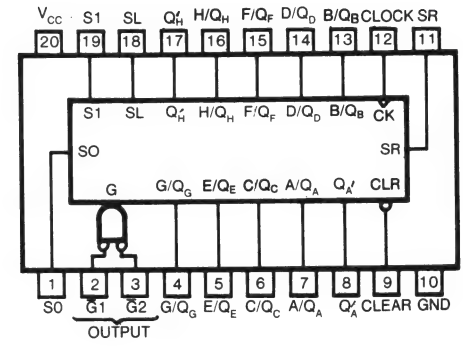
GD54/74LS299

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

Features

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operation:
  Hold (Store) Shift Left
  Shift Right Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- Applications:
  Stacked or Push-Down Registers.
  Buffer Storage, and
  Accumulator Registers

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

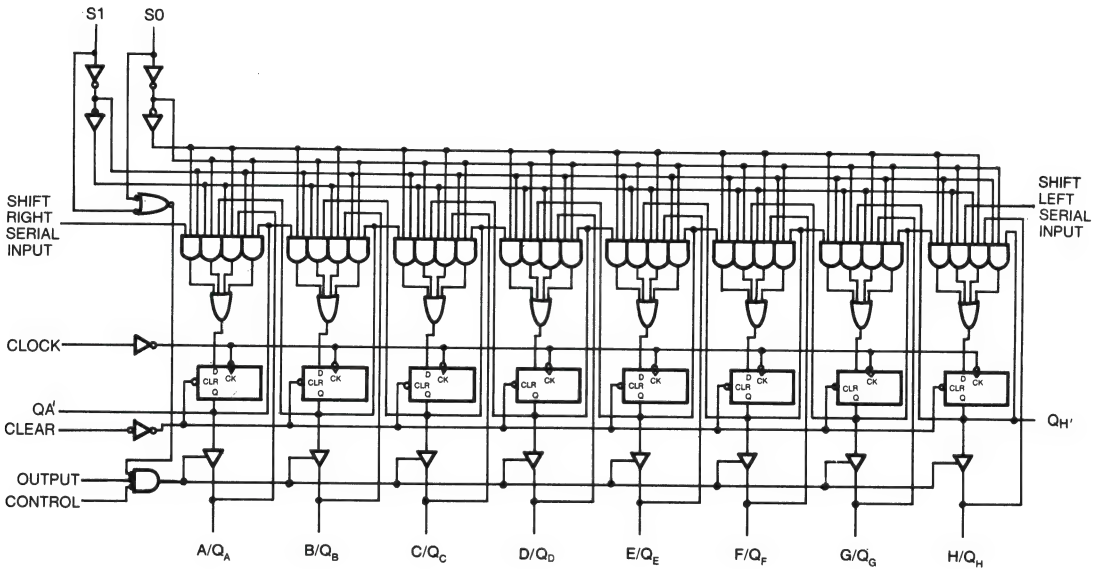
Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

Function Table

MODE	INPUTS								INPUTS/OUTPUTS								OUTPUT	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROOL		CLOCK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$*	$\overline{G2}$*		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}	Q_{EO}	Q_{FO}	Q_{GO}	Q_{HO}	Q_{AO}	Q_{HO}
	H	X	X	L	L	L	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}	Q_{EO}	Q_{FO}	Q_{GO}	Q_{HO}	Q_{AO}	Q_{HO}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

* When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however. sequential operation or clearing of the register is not affected.

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAHETER		54LS299 MIN	54LS299 NOM	54LS299 MAX	74LS299 MIN	74LS299 NOM	74LS299 MAX	UNIT
V_{CC}	Supply voltage,		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current,	Q_A thru Q_H			−1			−2.6	mA
		Q_A or Q_H			−0.4			−0.4	
I_{OL}	Low-level output current,	Q_A thru Q_H			12			24	mA
		Q_A or Q_H			4			8	
f_{clock}	Clock frequency,		0		25	0		25	MHz
$t_{w(clock)}$	Width of clock pulse,	Clock high	30			30			ns
		Clock low	10			10			
$t_{w(clear)}$	Width of clear pulse	Clear low	20			20			ns
t_{su}	Setup time,	Select	35↑			35↑			ns
		High-level data	20↑			20↑			
		Low-level data	20↑			20↑			
		Clear inactive-state	20↑			20↑			
t_h	Hold time,	Select	10↑			10↑			ns
		Data	0↑			0↑			
T_A	Operating free-air temperature,		−55		125	0		70	°C

* Data includes the two serial inputs and the eight input output data lines.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2.0			V
V_{IL}	Low-level input voltage				54			0.7	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=MIN,	I_I=−18mA				−1.5	V
V_{OH}	High-level output voltage	Q_A thru Q_H	V_{CC}=MIN, V_{IL}=MAX	V_{IH}=2V, I_{OH}=MAX	54	2.4	3.2		V
					74	2.4	3.1		
		$Q_{A'}$ or $Q_{H'}$			54	2.5	3.4		
					74	2.7	3.4		
V_{OL}	Low-level output voltage	Q_A thru Q_H	V_{CC}=MIN, V_{IL}=MAX, V_{IH}=MIN	I_{OL}=12mA	54,74		0.25	0.4	V
				I_{OL}=24mA	74		0.35	0.5	
		$Q_{A'}$ or $Q_{H'}$		I_{OL}=4mA	54,74		0.25	0.4	
				I_{OL}=8mA	74		0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Q_A thru Q_H	V_{CC}=MAX, V_O=2.7V	V_{IH}=2V				40	μA
I_{OZL}	Off-state output current low-level voltage applied	Q_A thru Q_H	V_{CC}=MAX, V_O=0.4V	V_{IH}=2V				−400	μA
I_I	Input current at maximum Input voltage	S0,S1	V_{CC}=MAX	V_I=7V				200	μA
		A thru H		V_I=5.5V				100	
		Any other		V_I=7V				100	
I_{IH}	High-level input current	A thru H, S0, S1	V_{CC}=MAX	V_I=2.7V				40	μA
		Any other						20	
I_{IL}	Low-level input current	S0, S1	V_{CC}=MAX	V_I=0.4V				−0.8	mA
		Any other						−0.4	
I_{OS}	Short-circuit output current	Q_A thru Q_H	V_{CC}=MAX (Note 2)			−30		−130	mA
		$Q_{A'}$ or $Q_{H'}$				−20		−100	
I_{CC}	Supply current		V_{CC}=MAX				33	53	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note3	25	35		MHz
t_{PLH}	Clock	Q_A' or Q_H'	$C_L=15$ pF $R_L=2$ kΩ See Note3		22	33	ns
t_{PHL}					26	39	
t_{PHL}	Clear	Q_A' or Q_H'			27	40	ns
t_{PLH}	Clock	Q_A thru Q_H	$C_L=45$ pF $R_L=665$ Ω See Note3		17	25	ns
t_{PHL}					26	39	
t_{PHL}	Clear	Q_A thru Q_H			26	40	ns
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H			13	21	ns
t_{PZL}					19	30	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	$C_L=5$ pF $R_L=665$ Ω See Note3		10	15	ns
t_{PLZ}					10	15	

* f_{max} = maximum clock frequency.
t_{PLH} = propagation delay time, low to-high-level output.
t_{PHL} = propagatio delay time, high-to-low-level output.
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level
Note 3: For testing f_{max} all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. See load circuits and waveforms on page 3-11.

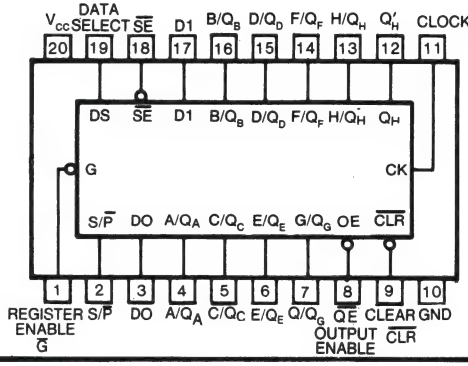
GD54/74LS322

8-BIT SHIFT REGISTERS WITH SIGN EXTEND

Feature

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- 3-State Outputs Drive Bus Lines Directly
- Sign Extend Function
- Direct Overriding Clear

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

These low-power Schottky eight-bit shift registers features multiplexed input/output data ports to achieve full eight-bit data handling in a single 20-pin package. Serial data may be entered into the shift-right register through either the D0 or the D1 input as selected by the data select input. A serial output (Q_H') is also provided to facilitate expansion. Synchronous parallel loading is accomplished by taking both the register enable and the S/$\overline{P}$ inputs low. This places the three-state input/output ports in the data input mode. Data are entered on the low-to-high transition of the clock. The data extend function repeats the sign in the Q_A flip-flop during shifting. A direct overriding clear input clears the internal registers when taken low whether the outputs are enabled or off. The output enable does not interfere with synchronous operation of the register.

Function Table

OPERATION	INPUTS							INPUTS/OUTPUTS				OUTPUT
	CLEAR $\overline{CLR}$	REGISTER ENABLE $\overline{G}$	S/$\overline{P}$	SIGN EXTEND $\overline{SE}$	DATA SELECT DS	OUTPUT ENABLE $\overline{OE}$	CLOCK	A/Q_A	B/Q_B	C/Q_C	H/Q_H	Q_H
Clear	L	H	X	X	X	L	X	L	L	L	L	L
	L	X	H	X	X	L	X	L	L	L	L	L
Hold	H	H	X	X	X	L	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{HO}	Q_{HO}
Shift Right	H	L	H	H	L	L	↑	DO	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
	H	L	H	H	H	L	↑	D1	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
Sign Extend	H	L	H	L	X	L	↑	Q_{An}	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
Load	H	L	L	X	X	X	↑	a	b	c	h	h

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state, however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/$\overline{P}$ input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
$Q_{A0}...Q_{H0}$ = the level of Q_A through Q_H, respectively, before the indicated steady state conditions were established
$Q_{An}...Q_{Hn}$ = the level of Q_A through Q_H, respectively, before the most recent ↑ transition of the clock
D0, D1 = the level of steady state inputs at inputs D0 and D1 respectively
a...h = the level of steady state inputs at inputs A through H respectively.

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Off-state output voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C t 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High Level Output Current	$Q_A \sim Q_H$	54			−1	mA
			74			−2.6	
		Q_H'	54			−0.4	
			74			−0.4	
I_{OL}	Low Level Ourput Current	$Q_A \sim Q_H$	54			12	mA
			74			24	
		Q_H'	54			4	
			74			8	
f_{clock}	Clock frequency			0		25	MHz
$t_{w(clock)}$	Width of clock pulse	clock high		30			ns
		clock low		10			
$t_{w(clear)}$	Width of clear pluse	clear low		20			ns
t_{su}	Set up time	Data select		10 ↑			ns
		High level data*		20 ↑			
		Low level data*		20 ↑			
		clear inactive state		20 ↑			
t_h	Hold time	Data select		10 ↑			ns
		Data*		0 ↑			
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

* Data includes the two serial inputs and the eight input/output data lines. ↑ The arrow indicates that the rising edge of the clock pulse is used for reference.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage				54			0.7	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level Output voltage	Q_A~Q_H	V_{CC}=Min V_{IL}=Max I_{OH}=Max V_{IH}=Min		54	2.4	3.2		V
					74	2.4	3.1		
		Q_H'			54	2.5	3.4		
					74	2.7	3.4		
V_{OL}	Low-level Output voltage	Q_A~Q_H	V_{CC}=Min V_{IH}=Min V_{IL}=Max	I_{OL}=12mA	54,74		0.25	0.4	V
				I_{OL}=24mA	74		0.35	0.5	
		Q_H'		I_{OL}=4mA	54,74		0.25	0.4	
				I_{OL}=8mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied	Q_A~Q_H	V_{CC}=Max, V_O=2.7V V_{IH}=Min,					40	μA
I_{OZL}	Off-state output current low-level voltage applied	Q_A~Q_H	V_{CC}=Max, V_O=0.4V V_{IH}=Min,					−400	μA
I_I	Input current at maximum input voltage	A~H	V_{CC}=Max	V_I=5.5V				0.1	mA
		Data Select		V_I=7V				0.2	
		Sign extend		V_I=7V				0.3	
		Any other		V_I=7V				0.1	
I_{IH}	High-level input current	A~H, DS	V_{CC}=Max, V_I=2.7V					40	μA
		Sign extend						60	
		Any other						20	
I_{IL}	Low-level input current	Data select	V_{CC}=Max V_I=0.4V					−0.8	mA
		Sign extend						−1.2	
		Any other						−0.4	
I_{OS}	Short-circuit output current	Q_A~Q_H	V_{CC}=Max (Note 2)			−30		−130	mA
		Q_H'				−20		−100	
I_{CC}	Supply current		V_{CC}=Max				35	60	mA

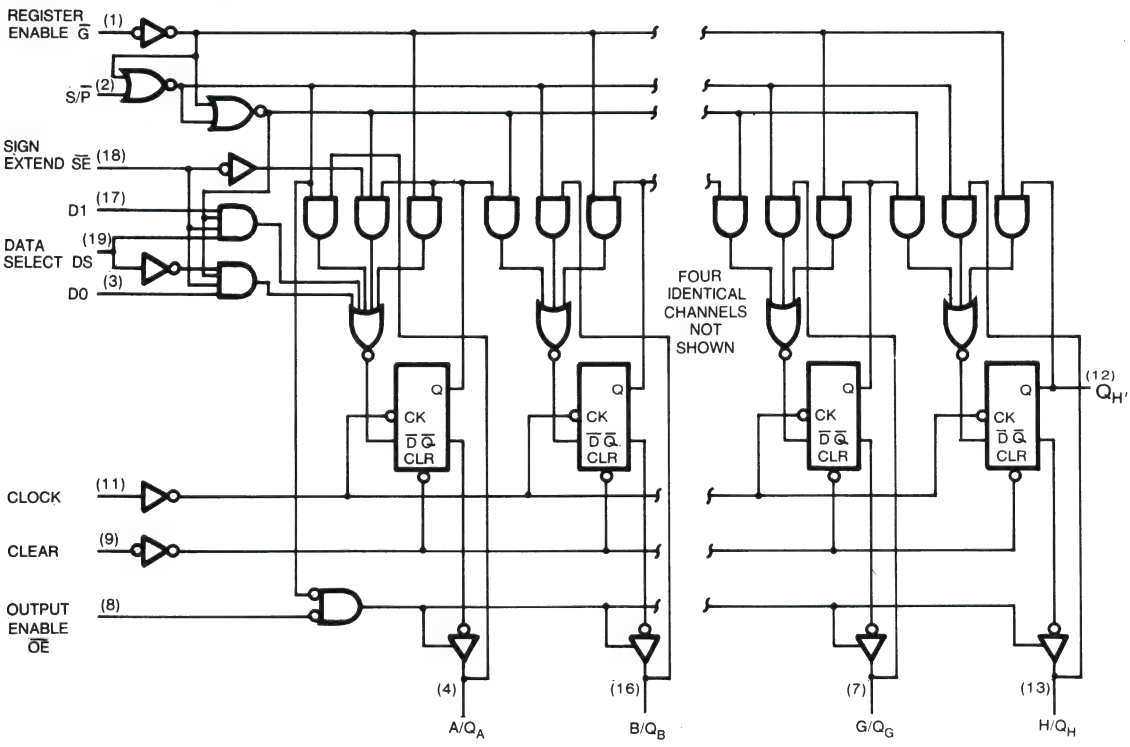
Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 1	20	35		MH_Z
t_{PLH}	Clock	Q_H'	$C_L=15pF$, $R_L=2K\Omega$		22	33	ns
t_{PHL}					26	35	
t_{PHL}	Clear	Q_H'			27	35	ns
t_{PLH}	Clock	Q_A thru Q_H	$C_L=45pF$, $R_L=665\Omega$		16	25	ns
t_{PHL}					22	33	
t_{PHL}	Clear	Q_A thru Q_H			22	35	ns
t_{PZH}	Output enable	Q_A thru Q_H			15	35	ns
t_{PZL}					15	35	
t_{PHZ}	Output disable	Q_A thru Q_H	$C_L=5pF$, $R_L=665\Omega$,		15	25	ns
t_{PLZ}					15	25	

Note 1: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.

Function Block Diagram



GD54/74LS365A

HEX-BUS DRIVERS; 3-STATE OUTPUTS, NON-INVERTED DATA OUTPUTS

Feature

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Choice of True or Inverting Outputs

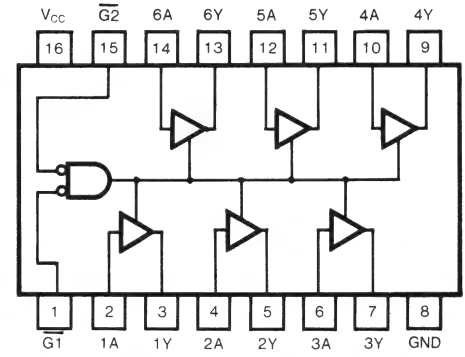
Description

These hex buffers and line drivers are designed specifically to improve both the performance and density of three state memory address drivers, clock drivers, and bus oriented receivers and transmitters. The desingers has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low control) inputs

Function Table

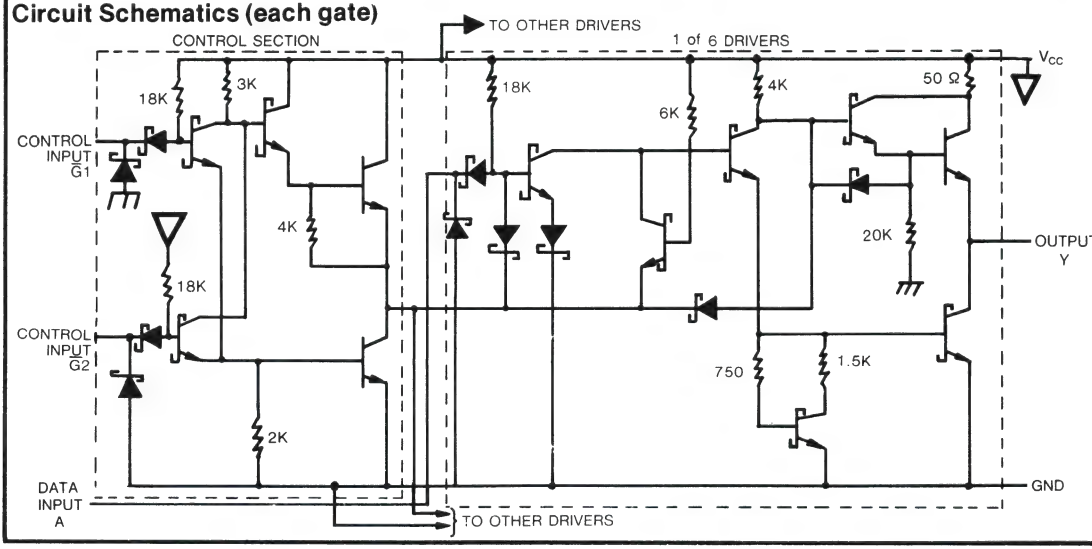
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	L	L
L	L	H	L
H	X	X	Z
X	H	X	Z

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Circuit Schematics (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Voltage applied to a disabled 3-state output 5.5V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−1	mA
		74			−2.6	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage				54			0.7	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage		V_{CC}=Min, V_{IL}=Max I_{OH}=Max, V_{IH}=Min		54	2.4	3.3		V
					74	2.4	3.1		
V_{OL}	Low-level output voltage		V_{CC}=Min V_{IL}=Max V_{IH}=Min	I_{OL}=12mA	54 74		0.25	0.4	V
				I_{OL}=24mA	74		0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	A inputs	V_{CC}=Max V_I=0.5V Either $\overline{G}$ inputs at 2V					−20	μA
			V_{CC}=Max V_I=0.4V Both $\overline{G}$ inputs at 0.4V					−0.4	mA
		$\overline{G}$ inputs	V_{CC}=Max V_I=0.4V					−0.4	mA
I_{OZH}	Off-state output current high-level voltage applied		V_{CC}=Max, V_O=2.4V V_{IH}=Min, V_{IL}=Max					20	μA
I_{OZL}	Off-state output current low-level voltage applied		V_{CC}=Max, V_O=0.4V V_{IH}=Min, V_{IL}=Max					−20	μA
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)			−40		−225	mA
I_{CC}	Supply current		V_{CC}=Max (Note 3)				14	24	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L=45pF$, $R_L=667\Omega$		10	16	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	22	ns
t_{PZL}	Output enable time to low level			19	35	ns
t_{PZH}	Output enable time to high level			24	40	ns
t_{PLZ}	Output disable time from low level	$C_L=5pF$, $R_L=667\Omega$			30	ns
t_{PHZ}	Output disable time from high level				35	ns

* t_{PLH} = propagation delay time, low-to-high-level output.
* t_{PHL} = propagation delay time, high-to-low-level output.
# For load circuit and voltage waveforms, see page 3-11.

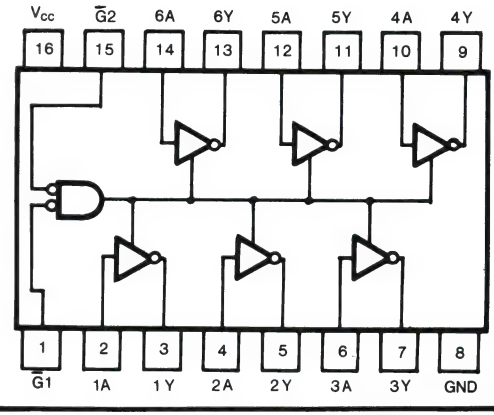
GD54/74LS366A

HEX 3-STATE INVERTING BUFFERS

Description

This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Pin Configuration



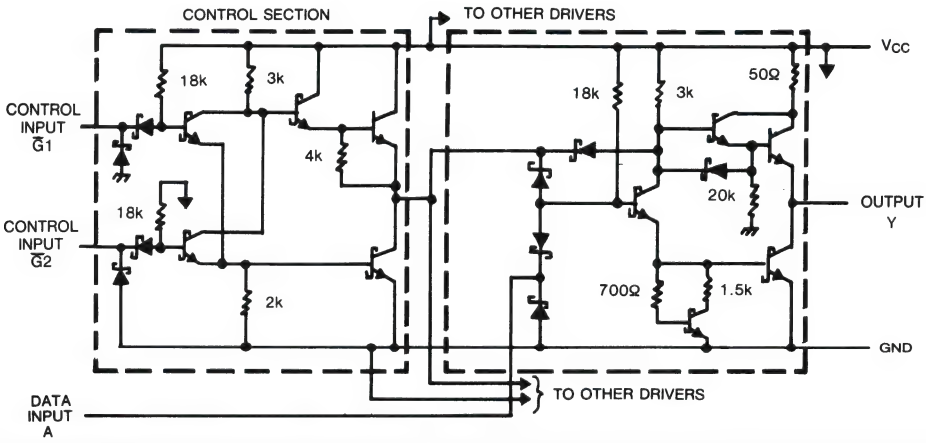
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Features

$Y = \overline{A}$

INPUT			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	L	H
L	L	H	L

Circuit Schematic (each buffer)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Off-state output voltage 5.5V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−1	mA
		74			−2.6	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage				54			0.7	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage		V_{CC}=Min, V_{IL}=Max		54	2.4	3.4		V
			I_{OH}=Max, V_{IH}=Min		74	2.4	3.1		
V_{OL}	Low-level output voltage		V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=12mA	54,74		0.25	0.4	V
				I_{OL}=24mA	74		0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	A inputs	V_{CC}=Max V_I=0.5V, Either $\overline{G}$ inputs at 2V					−20	μA
			V_{CC}=Max V_I=0.4V, Both $\overline{G}$ inputs at 0.4V					−0.4	mA
		$\overline{G}$ inputs	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OZH}	Off-state output current high-level voltage applied		V_{CC}=Max, V_O=2.4V, V_{IH}=Min, V_{IL}=Max					20	μA
I_{OZL}	Off-state output current low-level voltage applied		V_{CC}=Max, V_O=0.4V, V_{IH}=Min, V_{IL}=Max					−20	μA
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)			−40		−225	mA
I_{CC}	Supply current		V_{CC}=Max (Note 3)				12	21	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time low-to-high-level output	$C_L=45pF$, $R_L=667\Omega$		7	15	ns
t_{PHL}	Propagation delay time high-to-low-level output			12	18	ns
t_{PZH}	Output enable time to high level			18	35	ns
t_{PZL}	Output enable time to low level			28	45	ns
t_{PHZ}	Output disable time from high level	$C_L=5pF$, $R_L=667\Omega$			32	ns
t_{PLZ}	Output disable time from low level				35	ns

#For load circuit and voltage waveforms, see page 3-11.

GD54/74LS367A

HEX BUS DRIVERS WITH 3-STATE OUTPUTS

Feature

- 3-State Outputs Drive Bus Line or Buffer Memory Address Registers
- Choice of True or Inverting Outputs

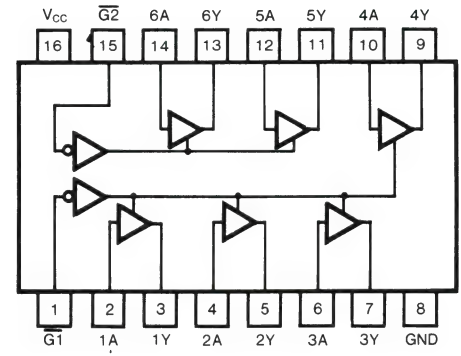
Description

These hex buffers and line drivers are designed specifically to improve both the performance and density of three state memory address drivers, clock drivers, and bus oriented receivers and transmitters. The designers has a choice of selected combinations of inverting and noniverting outputs, symmetrical $\overline{G}$ (active-low control) inputs.

Function Table

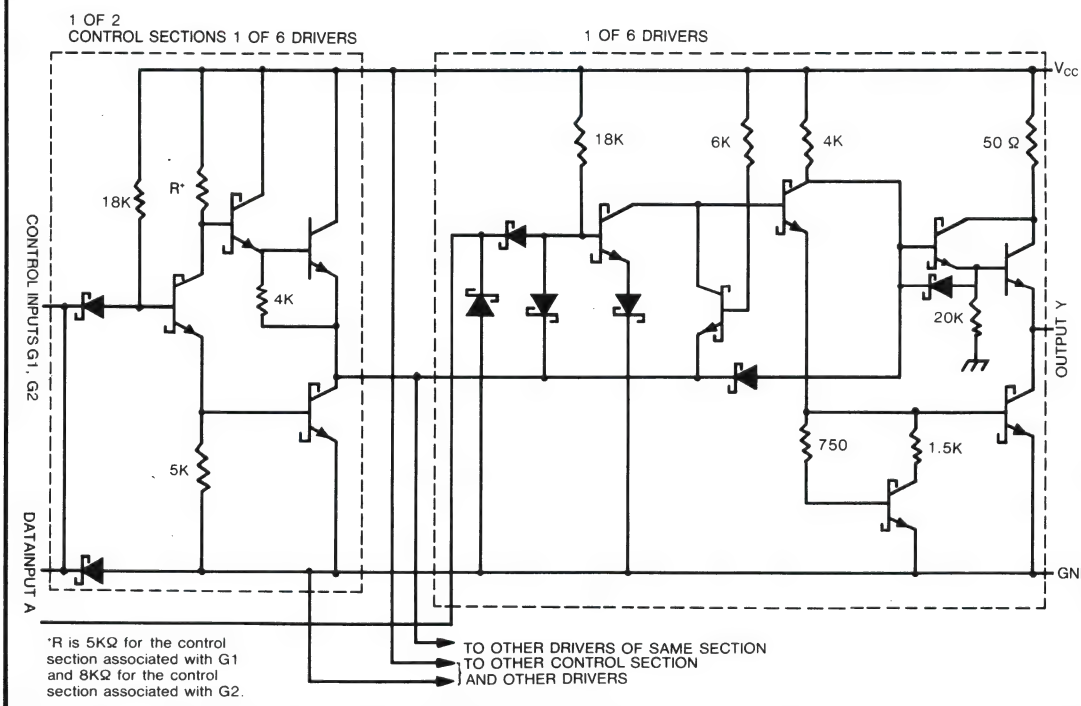
A	$\overline{G}$	Y
L	L	L
H	L	H
X	H	Z

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Schematic



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Voltage applied to a disabled 3-state output 5.5V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−1	mA
		74			−2.6	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min		54	2.4	3.4		V
				74	2.4	3.1		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=12mA	54,74		0.25	0.4	V
			I_{OL}=24mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	A inputs	V_{CC}=Max V_I=0.5V Either $\overline{G}$ inputs at 2V				−20	μA
			V_{CC}=Max V_I=0.4V Both $\overline{G}$ inputs at 0.4V				−0.4	mA
		$\overline{G}$ inputs	V_{CC}=Max V_I=0.4V				−0.4	mA
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.4V, V_{IH}=Min, V_{IL}=Max					20	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.4V, V_{IH}=Min, V_{IL}=Max					−20	μA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−40		−225	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				14	24	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L=45pF$, $R_L=667\Omega$		10	16	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	22	ns
t_{PZL}	Output enable time to low level			24	40	ns
t_{PZH}	Output enable time to high level			19	35	ns
t_{PLZ}	Output disable time from low level	$C_L=5pF$, $R_L=667\Omega$			35	ns
t_{PHZ}	Output disable time from high level				30	ns

For load circuit and voltage waveforms, see page 3-11.

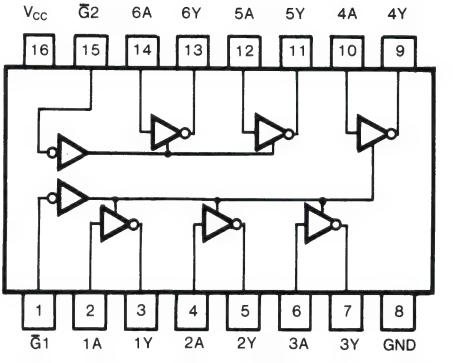
GD54/74LS368A

HEX TRI-STATE INVERTING BUFFERS

Description

This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus lines. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Pin Configuration

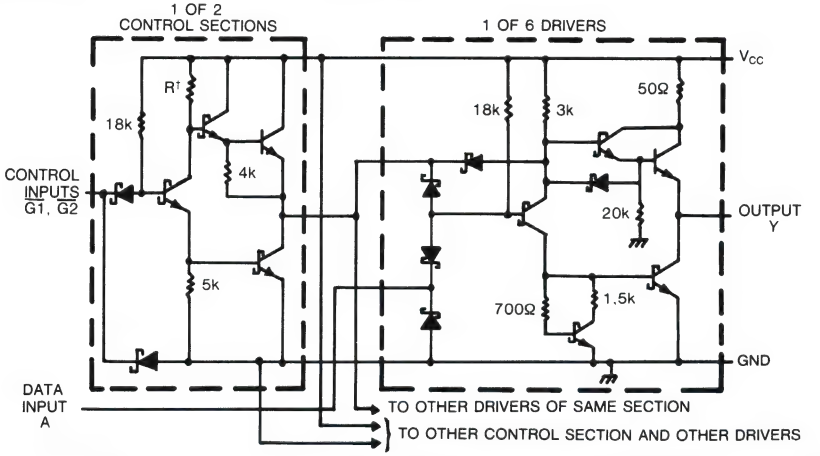


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

Input		Output
A	$\overline{G}$	Y
L	L	H
H	L	L
X	H	Z

Circuit Schematics (each buffer)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−1	mA
		74			−2.6	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage				54			0.7	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage		V_{CC}=Min, V_{IL}=Max I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
					74	2.7	3.1		
V_{OL}	Low-level output voltage		V_{CC}=Min V_{IL}=Max V_{IH}=Min	I_{OL}=12mA	54, 74		0.25	0.4	V
				I_{OL}=24mA	74		0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	A inputs	V_{CC}=Max V_I=0.5V Either $\overline{G}$ iputs at 2V					−20	μA
			V_{CC}=Max V_I=0.4V Both $\overline{G}$ inputs at 0.4V					−0.4	mA
		$\overline{G}$ inputs	V_{CC}=Max V_I=0.4V					−0.4	mA
I_{OZH}	Off-state output current high-level voltage applied		V_{CC}=Max, V_O=2.4V V_{IH}=Min, V_{IL}=Max					20	μA
I_{OZL}	Off-state output current low-level voltage applied		V_{CC}=Max, V_O=0.4V V_{IH}=Min, V_{IL}=Max					−20	μA
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)			−40		−225	mA
I_{CC}	Supply current		V_{CC}=Max (Note 3)				12	21	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should ot not exceed one second.
Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L=45pF$, $R_L=667\Omega$		7	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	18	ns
t_{PZH}	Output enable time to high level			18	35	ns
t_{PZL}	Output enable time to low level			28	45	ns
t_{PHZ}	Output disable time from high level	$C_L=5pF$, $R_L=667\Omega$			32	ns
t_{PLZ}	Output disable time from low level				35	ns

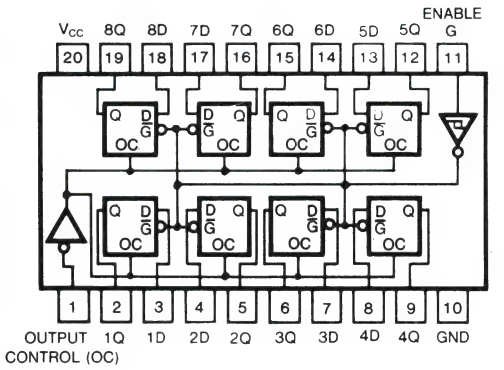
#For load circuit and voltage waveforms, see page 3-11.

GD54LS373/GD74LS373
OCTAL D-TYPE LATCHES; 3-STATE
OUTPUTS COMMON OUTPUT CONTROL COMMON ENABLE

Feautre

- 8 Latches in a Single Package
- 3-State Bus-Driving Outputs
- Full Paralle-Access for Loading
- Buffered Control Inputs
- Clock/Enable input Has Hysteresis to Improve Noise Rejection
- P-N-P Inputs Reduce D-C Loading on Data Lines

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the LS373 are transparent D-type latches. While the enable (G) is high the Q outputs will follow the data (D) inputs, when the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

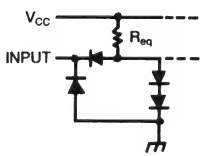
The output control does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

Function Table (Each Latch)

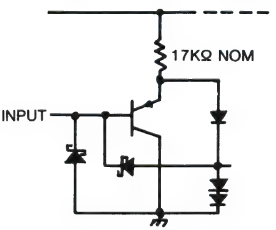
INPUTS			OUTPUT Q
OC	ENABLE G	D	
L	H	H	H
L	H	L	L
L	L	X	Q_O
H	X	X	Z

Schematic of Inputs and Outputs

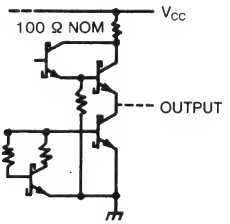
EQUIVALENT OF DATA INPUTS



EQUIVALENT OF ENABLE AND OUTPUT CONTROL INPUTS



TYPICAL OF ALL OUTPUTS



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Off-state output voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−1	mA
		74			−2.6	
t_w	Width of clock/enable pulse	High	15			ns
		Low	15			
t_{su}	Data setup time		5↓			ns
t_h	Data hold time		20↓			ns
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max, V_{IL}=Max, V_{IH}=Min		54	2.4	3.4		V
				74	2.4	3.1		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=12mA	54,74		0.25	0.4	V
			I_{OL}=24mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.7V, V_{IH}=Min, V_{IL}=Max					20	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.4V, V_{IH}=Min, V_{IL}=Max					−20	μA
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−30		−130	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				24	40	mA

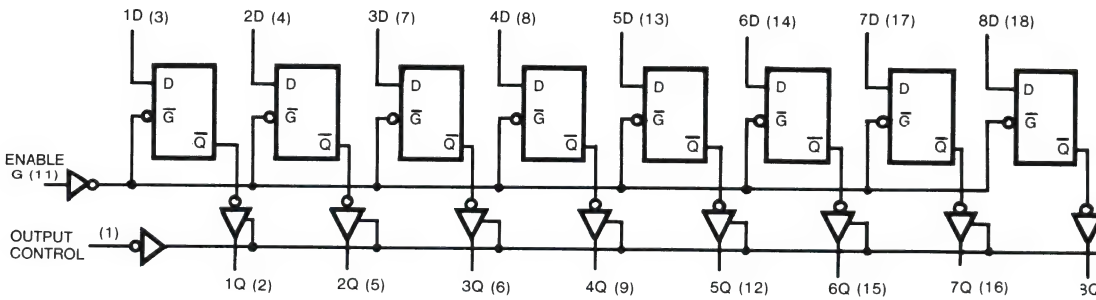
Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Any Q	$C_L=45pF$, $R_L=667\Omega$ See Note 1		12	18	ns
t_{PHL}					12	18	
t_{PLH}	Clock or enable	Any Q			20	30	ns
t_{PHL}					18	30	
t_{PZH}	Output control	Any Q			15	28	ns
t_{PZL}					25	36	
t_{PHZ}	Output control	Any Q	$C_L=5pF$, $R_L=667\Omega$		12	20	ns
t_{PLZ}					15	25	

*f_{max}=maximum clock frequency; tested with all outputs loaded.
t_{PLH}=propagation delay time, low-to-high-level output.
t_{PHL}=propagation delay time, high-to-low-level output.
t_{PZH}=output enable time to high level.
t_{PZL}=output enable time to low level.
t_{PHZ}=output disable time from high level.
t_{PLZ}=output disable time from low level.
Note 1: Maximum clock frequency is tested with all outputs loaded.
#For load circuit and voltage waveforms, see page 3-11.

Function Block Diagram



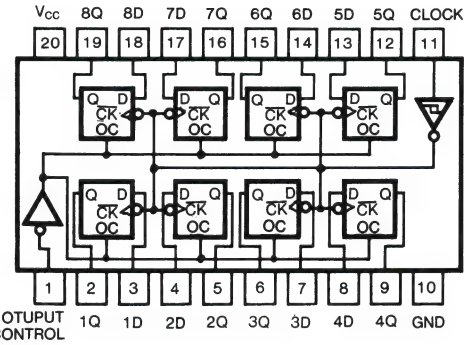
GD54/74LS374

OCTAL D TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

Feature

- D-Type-Flops in a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

These 8-bit flip-flops feature three-state outputs designed specifically for driving high capacitive or relatively low-impedance loads. This is particulaly suitable for implementing buffer registers, I/O port, bidirectional bus drivers, and working registers.

The eight flip-flops of the LS374 are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs will be set to the logic levels that were set up at the D inputs.

A buffered output-control input can be used to place the eight ouitputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull up components.

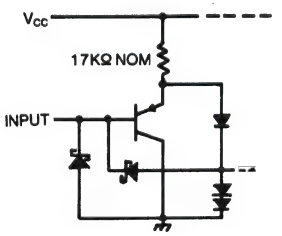
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Function Table

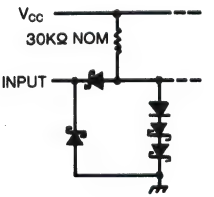
OUTPUT CONTROL	CLOCK (CK)	D	OUTPUT Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_O
H	X	X	Z

Schematic of Inputs and Outputs

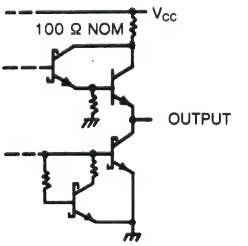
EQUIVALENT OF CLOCKS AND OUTPUT CONTROL INPUTS



EQUIVALENT OF DATA INPUTS



TYUPICAL OF ALL OUTPUTS



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Off-state output voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−1	mA
		74			−2.6	
t_w	Width of clock/enable pulse	High	15			ns
		Low	25			
t_{su}	Data setup time		20↑			ns
t_h	Data hold time		0↑			ns
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max, V_{IH}=Min	54	2.4	3.4		V
				74	2.4	3.1		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=12mA	54,74		0.25	0.4	V
			I_{OL}=24mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.7V, V_{IH}=Min, V_{IL}=Max					20	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.4V, V_{IH}=Min, V_{IL}=Max					−20	μA
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−30		−130	mA
I_{CC}	Supply current	V_{CC}=Max (Output control at 4.5V)				27	40	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

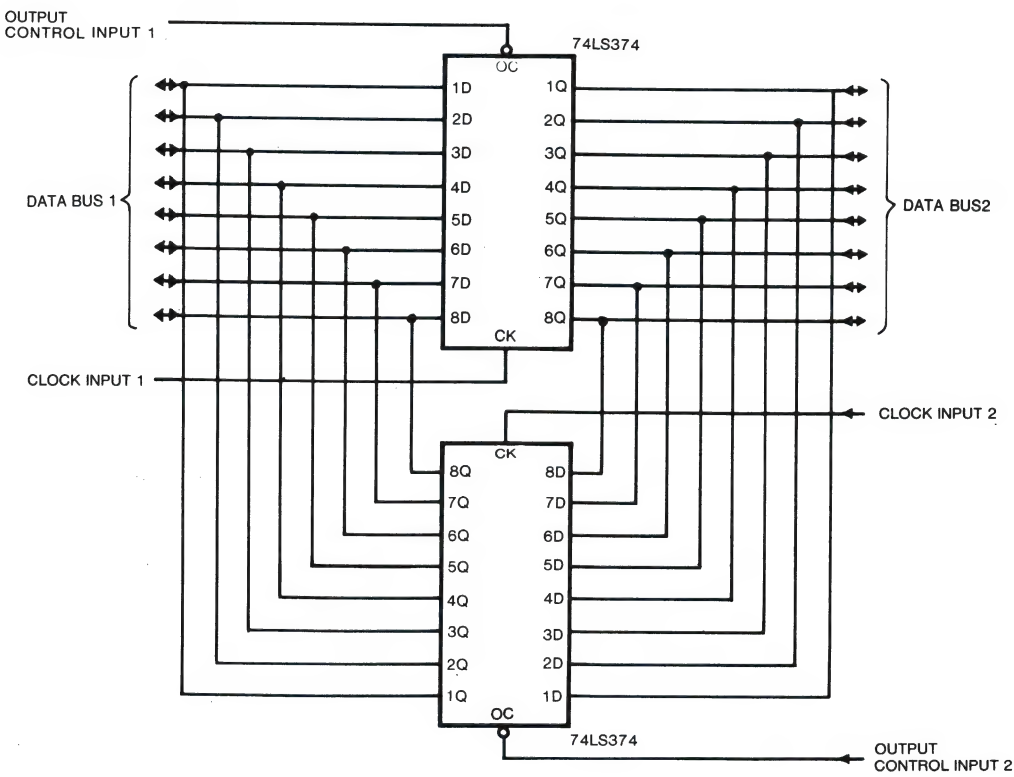
PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}			$C_L=45pF$, $R_L=667\Omega$ See Note 1	25	35		MHz
t_{PLH}	Clock or enable	Any Q			15	28	ns
t_{PHL}					19	28	
t_{PZH}	Output control	Any Q			20	28	ns
t_{PZL}					21	28	
t_{PHZ}	Output control	Any Q	$C_L=5pF$, $R_L=667\Omega$		12	20	ns
t_{PLZ}					14	25	

*f_{max}=maximum clock frequency; tested with all outputs loaded.
t_{PLH}=propagation delay time, low-to-high-level output.
t_{PHL}=propagation delay time, high-to-low-level output.
t_{PZH}=output enable time to high level.
t_{PZL}=output enable time to low level.
t_{PHZ}=output disable time from high level.
t_{PLZ}=output disable time from low level.

Note 1: Maximum clock frequency is tested with all outputs loaded.
#For load circuit and voltage waveforms, see page 3-11.

Application Example

8-BIT SHIFT REGISTER



GD54/74LS377

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH ENABLE

Features

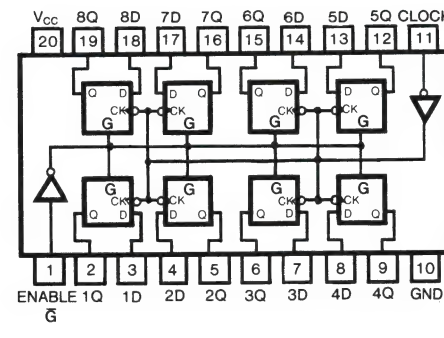
- Eight-bit, high speed parallel registers
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common clock enable

Description

This device contains 8 edge-triggered D-type flip-flop circuits and it is provided with clock input and enable input $\overline{G}$ common to all 8 circuits. When CK changes in each flip-flop from low to high, the data input signal D immediately before the change appears in output Q.

When $\overline{G}$ is set high, the output status does not change irrespective of the status of the other input signals. Malfunctioning does not result even if $\overline{G}$ is set from high to low or from low to high.

Pin Configuration



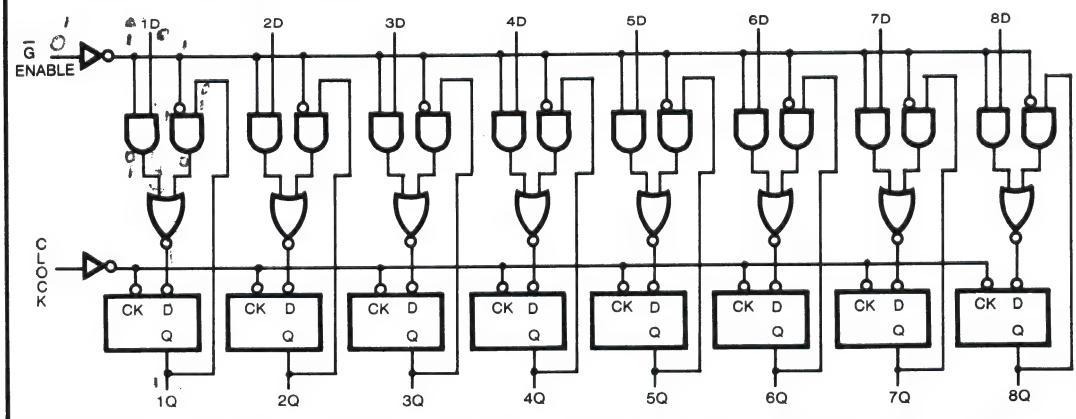
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (Note 1)

$\overline{G}$	CK	D	Q
H	X	X	Q^0
L	↑	H	H
L	↑	L	L
X	L	X	Q^0

Note 1 ↑ : Transition for low to high (positive edge trigger)
Q^0 : Level of Q before the indicated stead-state input conditions were established.
X : Irrelevant

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
f_{clock}	Clock frequecy		0		30	MHz
t_w	Width of clock or clear pulse		20			ns
t_{su}	Set up time	Data input	20↑			ns
		Enable active-state	25↑			
		Enable inactive-state	10↑			
t_h	Hold time	Data and Enable	5↑			ns
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min		54	2.5	3.5		V
				74	2.7	3.5		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				17	28	mA

Note 1: All typical Values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should ot not exceed one second.
Note 3: With all outputs open and ground applied to all data and enable inputs, I_{CC} is measured after a momentary ground, then 4.5V, is applied to clock.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	$C_L=15pF$, $R_L=2k\Omega$	30	40		MHz
t_{PHL}	Propagation delay time, high-to-low-level outputs from clock			18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level outputs from clock			17	27	ns

#For load circuit and voltage waveforms, see page 3-11.

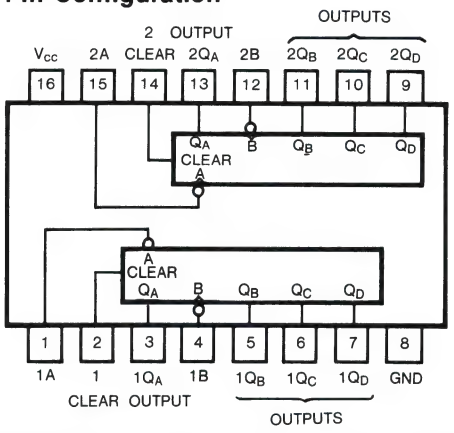
GD54/74LS390

DUAL 4-BIT DECADE AND BINARY COUNTERS

Features

- Dual Versions of the Popular 'LS90
- 'LS390... Individual Clocks for A and B Flip-Flops Provide Dual ÷ 2 ÷ 5 and Counters
- Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Version Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency...35MHz
- Buffered Output Reduce Possibility of Collector Commutation

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

Each of these monolithic circuits contains eight masterslave flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'LS390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The 'LS390 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing singals.

Function Table

BCD COUNT SEQUENCE (EACH COUNTER) (See Note A)

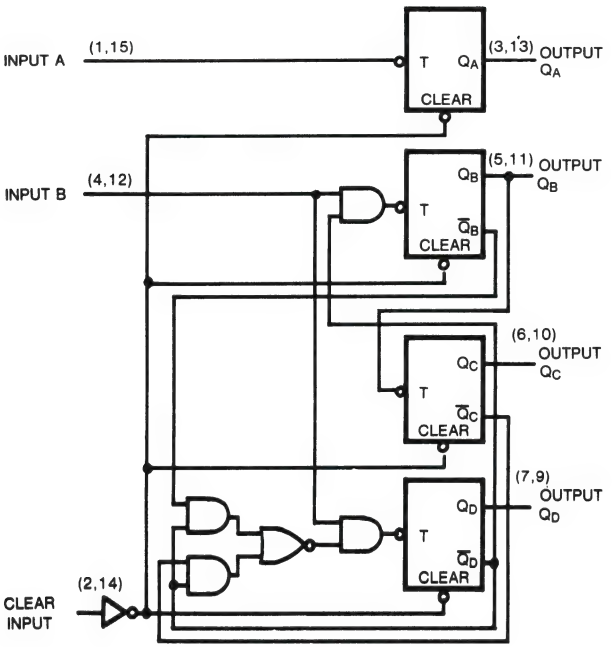
Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2) (EACH COUNTER) (See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	H
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Note A: Output Q_A is connected to input B for BCD count
B: Output Q_D is connected to input A for bi-quinary count
C: H=high level. L=low level

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage Clear 7V
  A or B 5.5V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54,74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{clock}	Clock frequency	A to Q_A		0		25	MHz
		B to Q_B		0		12.5	
t_W	Pulse Width	A		20			ns
		B		40			
		Clear High		20			
t_{su}	Clear inactive-state set up time			25↓			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min V_{IL}=Max		54	2.4	3.4		V
		I_{OH}=Max V_{IH}=Min		74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max V_I=7V	Clear				0.1	mA
		V_{CC}=Max V_I=5.5V	A				0.2	
			B				0.4	
I_{IH}	High-level input current	V_{CC}=Max V_I=2.7V	Clear				20	μA
			A				100	
			B				200	
I_{IL}	Low-level input current	V_{CC}=Max V_I=0.4V	Clear				−0.4	mA
			A				−1.6	
			B				−2.4	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				15	26	mA

Note 1: All typical values are at V_{CC}=V, T_A=25°C
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} measured with all outputs open, both CLEAR inputs grounded following momentary connection to 4.5 and all other inputs grounded.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER	TEST (INPUT)	TO (OUTPUT)	CONDITION#	MIN	TYP	MAX	UNIT
f_{max}	A	Q_A	$C_L=15pF$, $R_L=2k\Omega$ See Fig. 1	25	35		MHz
	B	Q_B		20	30		
t_{PLH}	A	Q_A			12	20	ns
t_{PHL}					13	20	
t_{PLH}	A	Q_C			37	60	ns
t_{PHL}					39	60	
t_{PLH}	B	Q_B			13	21	ns
t_{PHL}					14	21	
t_{PLH}	B	Q_C			24	39	ns
t_{PHL}					26	39	
t_{PLH}	B	Q_D			13	21	ns
t_{PHL}					14	21	
t_{PHL}	Clear	Any			24	39	ns

#For load circuit and voltage waveforms, see page 3-11.

PARAMETER MEASUREMENT INFORMATION

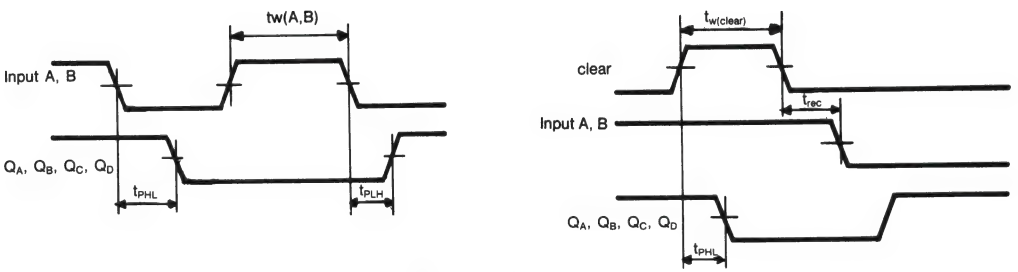


Fig 1 Voltage Waveforms

GD54/74LS393

DUAL 4-BIT BINARY COUNTERS

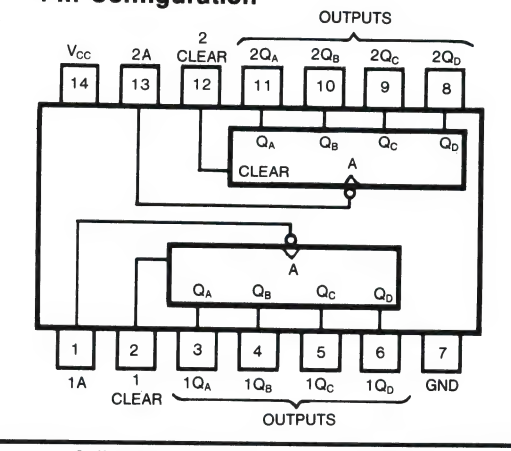
Feature

- Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency ... 35 MHz

Description

Each of this monolithic circuit contains eight master slave flip-flops and additional gating to implement two individual four-bit counters in a single package. It comprises two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide by 256. It has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Pin Configuration

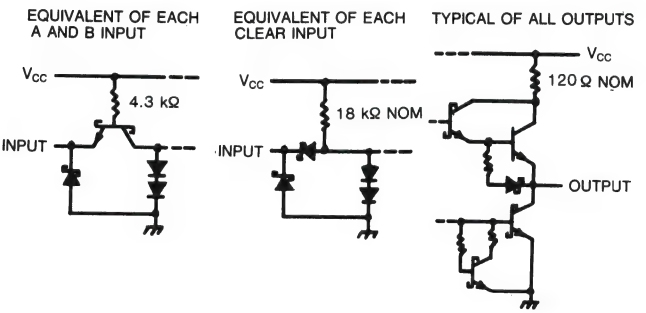


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

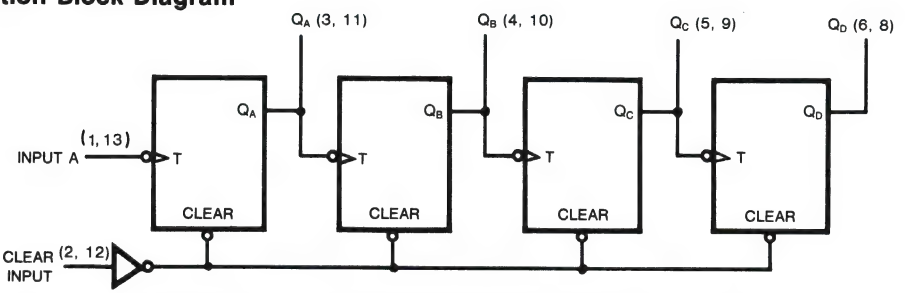
Count Sequence (Each Counter)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Schematics of Inputs and Outputs



Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Clear input voltage 7V
- Any A or B clock input voltage 5.5V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54,74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{COUNT}	Count frequency	A input		0		25	MHz
t_w	Pulse with	A input high or low		20			ns
		Clear high		20			
t_{SU}	Clear inactive-state setup time			25↓			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

↓ The arrow indicates the falling edge of the clock pulse is used for reference.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	Typ (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	CLEAR				0.1	mA
			INPUT A				0.2	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	CLEAR				20	μA
			INPUT A				100	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	CLEAR				−0.4	mA
			INPUT A				−1.6	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				15	26	mA

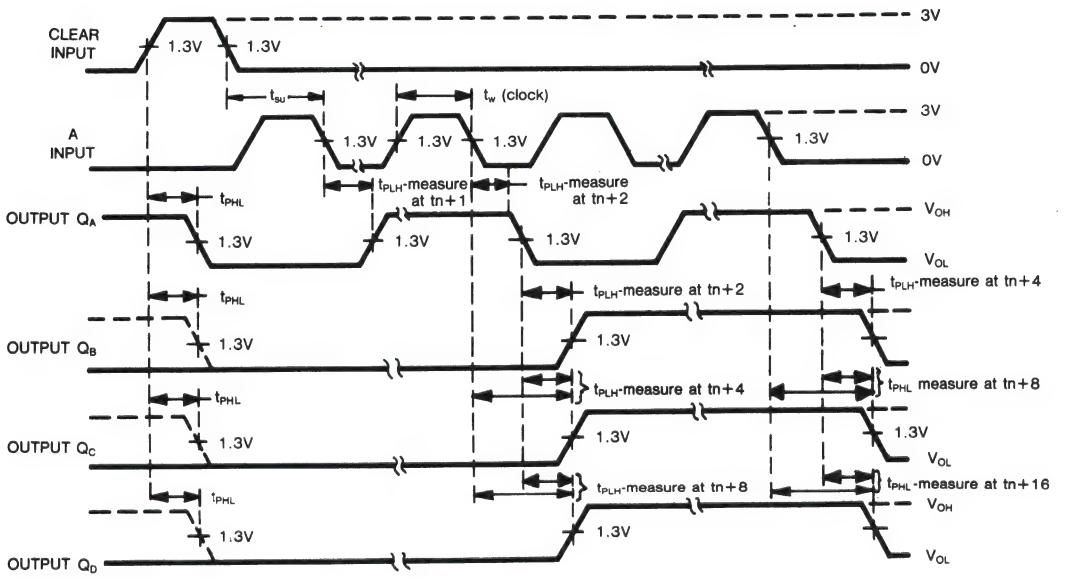
Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}	A	Q_A	$C_L=15pF$, $R_L=2k\Omega$ See Fig. 1	25	35		MHz
t_{PLH}	A	Q_A			12	20	ns
t_{PHL}					13	20	
t_{PLH}	A	Q_D			40	60	ns
t_{PHL}					40	60	
t_{PHL}	Clear	Any			24	39	ns

#For load circuit and voltage waveforms, see page 3-11.
*f_{max}=maximum count frequency
t_{PLH}=propagation delay time low-to-high-level output
t_{PHL}=propagation delay time high-to-low-level output

Parameter Measurement Information



Note A: Input pulses are supplied by a generator having the following characteristic $t_r \leq 15ns$, $t_f \leq 6ns$, PRR≤1 MHz, duty cycle=50%, $Z_{out} \approx 50$ ohms.

Figure 1 Voltage Waveforms.

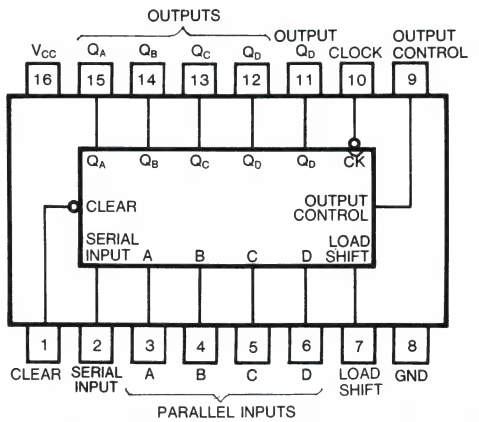
GD54/74LS395A

4-BIT UNIVERSAL SHIFT REGISTERS; 3 STATE OUTPUT

Feature

- Three-State, 4 Bit, Cascadable, Parallel-In, Parallel-Out Registers
- Low Power Dissipation ... 75mW Typical (Enable)
- Applications: N-Bit Serial-to-Parallel Converter
  N-Bit Parallel-to-Serial Converter
  N-Bit Storage Register

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

This 4-bit register features parallel inputs, parallel outputs, cascadable output, and clock, serial load/shift, output control, and direct overriding clear inputs.

Shifting is accomplished when the load/shift control is low. Parallel loading is accomplished by applying the four bits of data and taking the load/shift control input high. The data are loaded into the associated flip-flops and appear at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

When the output control is low, the nomal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently of the level of the clock by a high logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected. During the high-imedance mode, the output at Q_D is still available for cascading.

Function Table

INPUT								3-STATE OUTPUTS				CASCADE OUTPUT
CLEAR	LOAD/SHIFT CONTROL	CLOCK	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D	Q_D
L	X	X	X	X	X	X	X	L	L	L	L	L
H	H	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}	Q_{DO}
H	H	↓	X	a	b	c	d	a	b	c	d	d
H	L	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}	Q_{DO}
H	L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}

When the output control is high, the 3-state outputs are disable to the high-impedance state; however, sequential operation of the registers and the output at Q_D are not affected.

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		GD54LS395A			GD74LS395A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current	Q_A, Q_B, Q_C, Q_D			−1			−2.6	mA
		Q'_D			−0.4			−0.4	
I_{OL}	Low-level output current	Q_A, Q_B, Q_C, Q_D			12			24	mA
		Q'_D			4			8	
f_{clock}	Clock frequency		0		30	0		30	MHz
$t_{w(clock)}$	Width of clock pulse		16			16			ns
t_{su}	Set up time, high-level or low-level data	Load/shift input	40			40			ns
		All other inputs	20			20			
t_h	Hold time, high-level or low-level data		10			10			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP	MAX (Note1)	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage							0.8	V
V_{IK}	Input clamp voltage		V_{CC}=4.75V, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V, I_{OH}=MAX		Q_A, Q_B, Q_C, Q_D	2.4	3.4		V
					Q'_D	2.7	3.4		
V_{OL}	Low-level output voltage	54,74	V_{CC}=4.75V, V_{IL}=0.8V, V_{IH}=2V	Q_A, Q_B	I_{OL}=12mA		0.25	0.4	V
		74		Q_C, Q_D	I_{OL}=24mA		0.35	0.5	
		54,74		Q_D	I_{OL}=4mA		0.25	0.4	
		74			I_{OL}=8mA		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied		V_{CC}=Max, V_{IH}=2V, V_O=2.7V		Q_A, Q_B, Q_C, Q_D			20	μA
I_{OZL}	Off-state output current low-level voltage applied		V_{CC}=Max, V_{IH}=2V, V_O=0.4V		Q_A, Q_B, Q_C, Q_D			−20	μA
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)		Q_A, Q_B, Q_C, Q_D	−30		−130	mA
					Q_D'	−20		−100	
I_{CC}	Supply current		V_{CC}=Max (Note 3)		Condition A		22	34	mA
					Condition B		21	31	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.

Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Note 3: I_{CC} is measured with the outputs open, the serial input and mode control at 4.5V, and the data inputs grounded under the conditions:

A. Output control at 4.5V and a momentary 3V, then ground, applied to clock input.

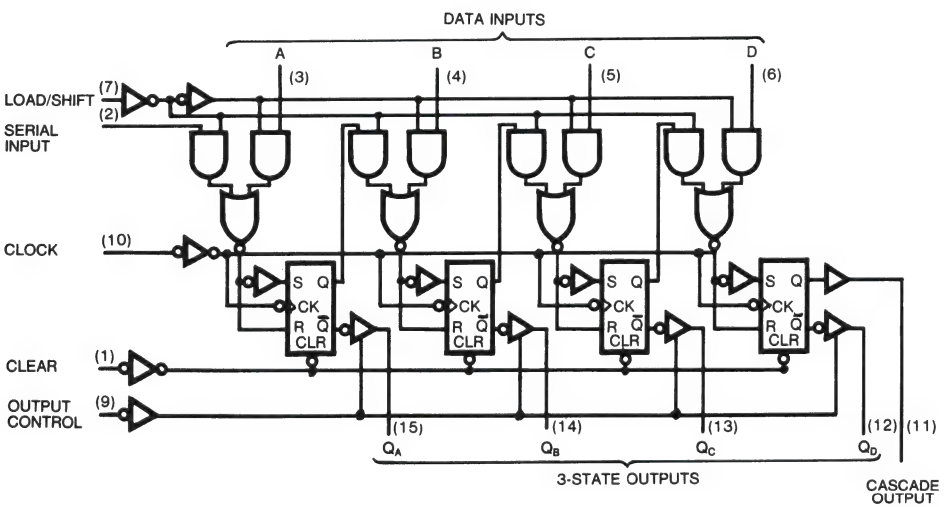
B. Output control and clock input grounded.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	Q_A, Q_B, Q_C, Q_D outptus ; $R_L=667\Omega$, $C_L=45pF$ Q_D' output ; $R_L=2k\Omega$, $C_L=15pF$	30	45		MHz
t_{PHL}	Propagation delay time, high-to-low-level outptu from clear			22	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output			15	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	30	ns
t_{PZH}	Output enable time to high level			15	25	ns
t_{PZL}	Output enable time to low level			17	25	ns
t_{PHZ}	Output disable time from high level	$C_L=5pF$		11	17	ns
t_{PLZ}	Oupput disable time from low level			12	20	ns

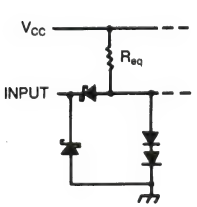
#For load circuit and voltage waveforms, see page 3-11.

Function Block Diagram



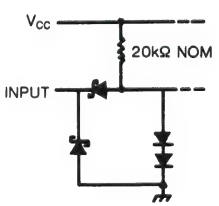
Sechmatics of Inputs and Outputs

EQUIVALENT OF SERIAL AND DATA INPUTS

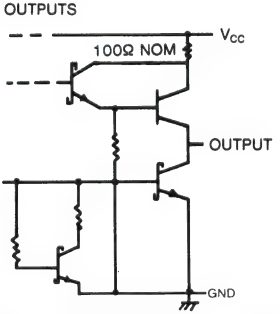


Serial: R_{eq}=30kΩ NOM
A.B.C.D: R_{eq}=20kΩ NOM

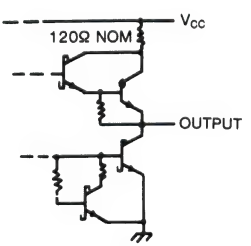
EQUIVALENT OF OTHER INPUTS



TYPICAL OF Q_A, Q_B, Q_C, Q_D OUTPUTS



TYPICAL OF Q_D, OUTPUTS



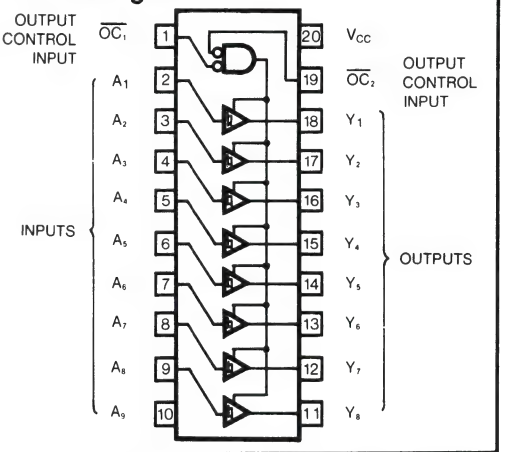
GD54/74LS541

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT(NONINVERTED)

Features

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins
- Data Flow-thru Pinout (All Inputs on Opposite Side from Outputs)
- High Fan Out (I_{OL}=24mA)
- Typical Power Dissipation (120mW)

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

The GD54/74LS541 is a semiconductor integrated circuit containing 1 buffer block with 3-state non-inverted outputs and is provided with output control inputs which are common to 8 circuits and which are independent.

When $\overline{OC_1}$ or $\overline{OC_2}$ is low, low appears in output Y if input A is low, and high appears in Y if A is high.

All outputs are set to the high-impedance state when $\overline{OC_1}$ and $\overline{OC_1}$ are in any other state.

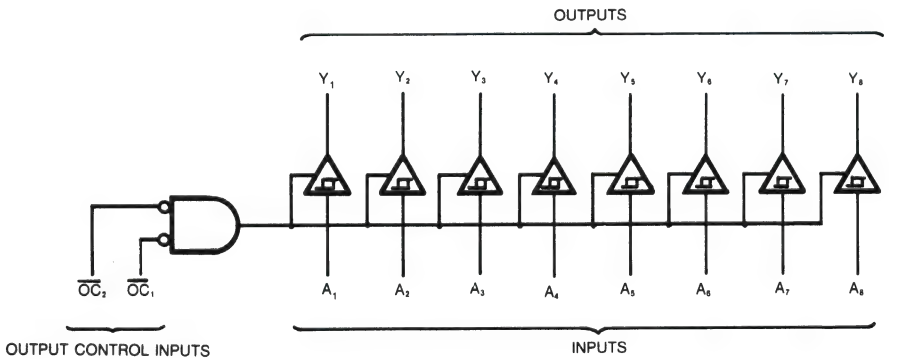
The input and output pins are arranged for facilitated board layout (data flow-thru pin out).

Function Table (Note 1)

A	$\overline{OC_1}$	$\overline{OC_2}$	Y
L	L	L	L
H	L	L	H
X	L	H	Z
X	H	L	Z
X	H	H	Z

Note 1 Z : High-impedance
X : Irrelevant

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage Any G 7V
  A or B 5.5V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−12	mA
		74			−15	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAETER	TEST CONDITION #	'LS541			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L=45pF$, $R_L=667\Omega$,		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	18	ns
t_{PZL}	Output enable time to low level			25	38	ns
t_{PZH}	Output enable time to high level			20	32	ns
t_{PLZ}	Output disable time from low level	$C_L=5pF$, $R_L=667\Omega$,		18	29	ns
t_{PHZ}	Output disable time from high level			10	18	ns

For load circuit and voltage waveforms, see page 3-11

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage				54			0.7	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage		V_{CC}=Min, V_{IH}=Min V_{IL}=Max, I_{OH}=−3mA		54, 74	2.4	3.4		V
			V_{CC}=Min, V_{IH}=Min V_{IL}=0.5V, I_{OH}=Max		54, 74	2			
V_{OL}	Low-level output voltage		V_{CC}=Min V_{IL}=Max V_{IH}=Min	I_{OL}=12mA	54, 74		0.25	0.4	V
				I_{OL}=24mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied		V_{CC}=Max, V_O=2.7 V_{IH}=Min, V_{IL}=Max,					20	μA
I_{OZL}	Off-state output current low-level voltage applied		V_{CC}=Max, V_O=0.4V V_{IH}=Min, V_{IL}=Max					−20	μA
I_I	Input current at maximun input voltage		V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.4V					−0.2	mA
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	Outputs high	V_{CC}=5.25V Outputs open				18	32	mA
		Outputs low					30	52	
		All outputs disabled					32	55	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

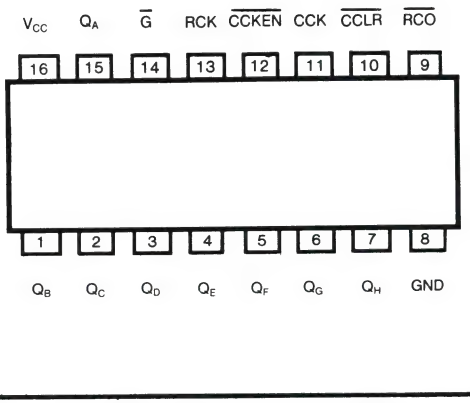
GD54/74LS590

8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

Features

- 8-Bit Counter with Register
- Parallel Register Outputs
- Counter has Direct Clear
- 3-State Outputs
- Guaranteed Counter Frequency .... DC to 20 MHz

Pin Configuration



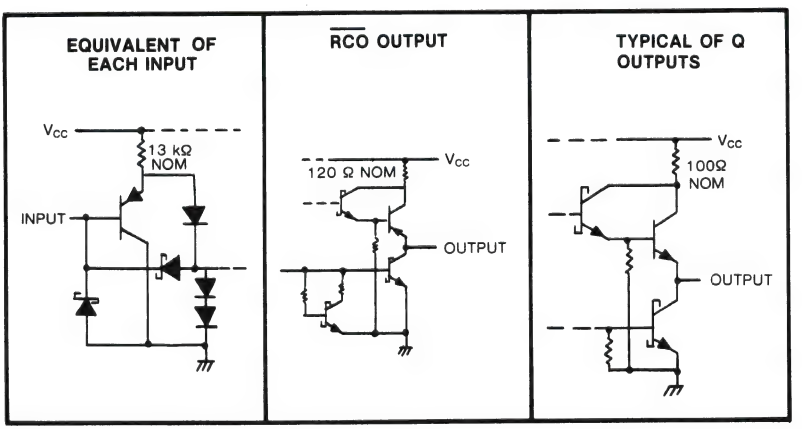
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

These devices contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading a ripple carry output $\overline{RCO}$ is provided. Expansion is easily accomplished by tying $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage, etc.

Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

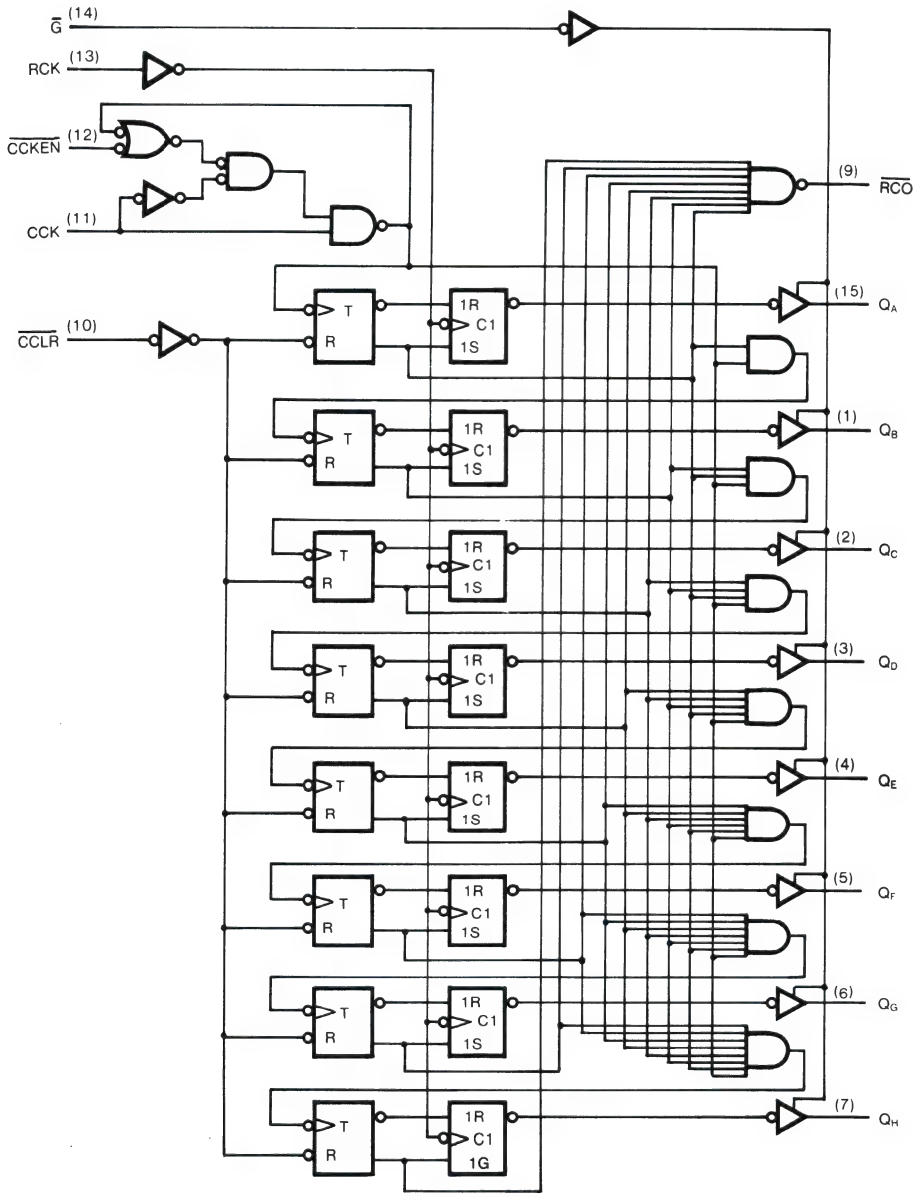
Schematics of Inputs and Outputs



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Off-state output voltage 5.5V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Function Block Diagram



Recommended Operating Conditions

SYMBOL	PARAMAETER		GD54LS MIN	GD54LS NOM	GD54LS MAX	GD74LS MIN	GD74LS NOM	GD74LS MAX	UNIT
V_{CC}	Supply voltage,		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current,	$\overline{RCO}$			−400			−400	μA
		Q			−1			−2.6	mA
I_{OL}	Low-level output current,	$\overline{RCO}$			8			16	mA
		Q			12			24	
f_{CCK}	Counter clock frequency,		0		20	0		20	MHz
$t_{W(CCK)}$	Width of counter clock pulse,		25			25			ns
$t_{w(CCLR)}$	Width of counter clear pulse,		20			20			ns
$t_{w(RCK)}$	Width of counter clear pulse,		20			20			ns
t_{enable}	Count enable time,	$\overline{CCKEN}$↓ to CCK↑	20			20			ns
t_{su}	Clear inactive-state setup time,	$\overline{CCLR}$↑ to CCK↑	20			20			ns
t_{su}	Setup time, (see Note 1)	CCK↑ to RCK↑	40			40			ns
T_A	Operating free-air temperature,		−55		125	0		70	°C

NOTE 1: This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage				54			0.7	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High Level Output Voltage	Q	V_{CC}=Min, V_{IL}=Max	I_{OH}=−1mA	54	2.4	3.2		V
				I_{OH}=−2.6mA	74	2.4	3.1		
		$\overline{RCO}$	V_{IH}=Min	I_{OH}=−1mA	54,74	2.4	3.2		
V_{OL}	Low Level Output Voltage	Q	V_{CC}=Min, V_{IH}=Min, V_{IL}=Max	I_{OL}=12mA	54,74		0.25	0.4	V
				I_{OL}=24mA	74		0.35	0.5	
		$\overline{RCO}$		I_{OL}=8mA	54,74		0.25	0.4	V
				I_{OL}=16mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied	Q	V_{CC}=Max, V_O=2.7V. V_{IH}=Min, V_{IL}=Max					20	μA
I_{OZL}	Off-stage output current low-level voltage applied	Q	V_{CC}=Max, V_O=0.4V V_{IH}=Min, V_{IL}=Max					−20	μA
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	CCK	V_{CC}=Max, V_I=0.4V					−0.8	mA
		Others						−0.2	
I_{OS}	Short-circuit output current	Q	V_{CC}=Max, V_O=0V (Note)			−30		−130	mA
		$\overline{RCO}$				−20		−100	
I_{CC}	Supply current		V_{CC}=Max (Note 3)	Outputs high			33	55	mA
				Outputs low			44	65	
				Output at high impedance			46	65	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Note more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
Note 3: All possible inputs grounded. All inputs open.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS #	LS590			UNIT
				MIN	TYP	MAX	
f_{max}	CCK	$\overline{RCO}$	$R_L=1k\Omega$, $C_L=30pF$	20	35		MHz
t_{PLH}	CCK↑	$\overline{RCO}$			15	22	ns
t_{PHL}	CCK↑	$\overline{RCO}$			20	30	ns
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$			30	45	ns
t_{PLH}	RCK↑	Q	$R_L=667\Omega$, $C_L=45pF$		12	18	ns
t_{PHL}	RCK↑	Q			22	33	ns
t_{PZH}	$\overline{G}$↓	Q			25	38	ns
t_{PZL}	$\overline{G}$↓	Q			30	45	ns
t_{PHZ}	$\overline{G}$↑	Q	$R_L=667\Omega$, $C_L=5pF$		20	30	ns
t_{PLZ}	$\overline{G}$↑	Q			25	38	ns

For load circuits and voltage wareforms, see page 3-11.

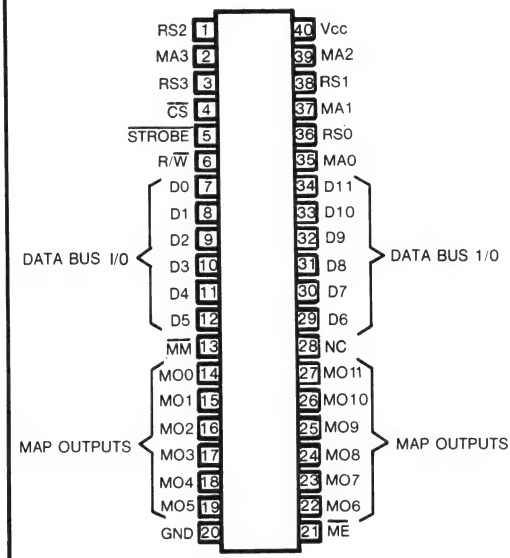
GD54/74LS612

MEMORY MAPPERS WITH 3-STATE MAP OUTPUTS

Feature

- Expands 4 Address Lines to 12 Address Lines
- Designed for Paged Memory Mapping

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Descriptions

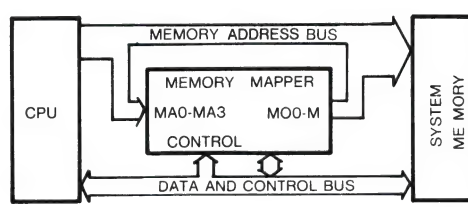
These memory-mapper integrated circuits contain a 4-line to 16-line decoder, a 16-word by 12-bit RAM, 16 channels of 2-line to 1-line multiplexers, and other miscellaneous circuitry on a monolithic chip.

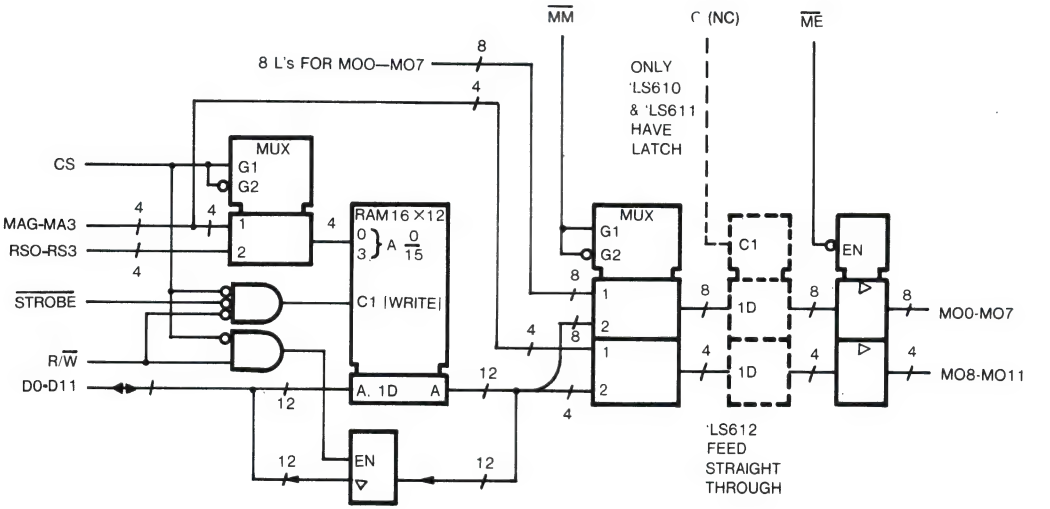
The memory mappers are designed to expand a microprocessor's memory address capability by eight bits. Four bits of the memory address bus (see the figure below) can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus through the map output buffers along with the unused memory address bits from CPU. However, addressable memory space without reloading the map registers is the same as would be available with the memory mapper left out. The addressble memory space is increased only by periodically reloading the map registers from the data bus.

This configuration lends itself to memory utilization of 16 pages of 2(n-4) registers each without reloading (n= number of address bits available from CPU).

These devices have four modes of operation (read, write, map, and pass). Data may be read from or loaded into the map register selected by the register select inputs (RS0 thru RS3) under control of R/$\overline{W}$ whenever chip select ($\overline{CS}$) is low. The data I/O takes place on the data bus D0 thru D7. The map operation will output the contents of the map register selected by the map address inputs (MA0 thru MA3) when $\overline{CS}$ is high and $\overline{MM}$ (map mode control) is low. The LS612 output stages are transparent in this mode.

When $\overline{CS}$ and $\overline{MM}$ are both high (pass mode), the address bits on MA0 thru MA3 appear at M08-M011, respectively, (assuming appropriate latch control) with low levels in the other bit positions of the map outputs.





'LS612 have 3-state (▽) map outputs.

PIN FUNCTION TABLE

PIN	PIN NAME	FUNCTIONAL DESCRIPTION
7-12, 29-34	D0 thru D11	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0-RS3 when $\overline{CS}$ is low. Mode controlled by R/$\overline{W}$.
36,38,1,3	RS0 thru RS3	Register select inptus for I/O operations.
6	R/$\overline{W}$	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
5	$\overline{STROBE}$	Strobe input used to enter data into the selected map register during I/O operations.
4	$\overline{CS}$	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
35,37,39,2	MA0 thru MA3	Map address inputs to select one of 16 map registers when in map mode ($\overline{MM}$ low and $\overline{CS}$ high)
14-19 22-27	MO0 thru MO11	Map outputs. Present the map register contents to the system memory address bus in the map mode. In the pass mode, these outputs provide the map address data on MO8-MO11 and low levels on MO0-MO7.
13	$\overline{MM}$	Map mode input. When low, 12 bits of data are transferred from the selected map register to the map outputs. When high (pass mode), the 4 bits present on the map address inputs MA0-MA3 are passed to the map outputs MO8-MO11, respectively, while MO0-MO7 are set low.
21	$\overline{ME}$	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
28	NC	No internal connection
40,20	Vcc,GND	5-V power supply and network ground (substrate) pins.

Note 1: Voltage values are with respect to network ground terminal.

Absolute Maximum Ratings

- Supply voltage, Vcc(see Notge 1) 7V
- Input voltage: Data Bus I/O 5.5V
  All other inputs 7V
- Operating free-air temperature range: GD54LS ..... −55°C to 125°C
  GD74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommend Operating Conditions

	PARAMETER		54LS612 MIN	NOM	MAX	74LS162 MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage,		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current,	MO			−12			−15	mA
		D			−1			−2.6	
I_{OL}	Low-level output current,	MO			12			24	mA
		D			4			8	
t_{SLSH}	Width of strobe input pulse,	See Figure 1	75			75			ns
t_{CSLSL}	CS setup time (CS low to strobe low),		20			20			ns
t_{WLSL}	R/W setup time (R/W low to strobe low),		20			20			ns
t_{RVSL}	RS setup time (RS valid to strobe low),		20			20			ns
t_{DVSH}	Data setup time (D0-D11 valid to strobe high),		75			75			ns
t_{SHCSH}	CS hold time (Strobe high to CS high),		20			20			ns
t_{SHWH}	R/W hold time (Strobe high to R/W high),		20			20			ns
t_{SHRX}	RS hold time (Strobe high to RS invalid),		20			20			ns
t_{SHDX}	Data hold time (Strobe high to D0-D11 invalid),		20			20			ns
T_A	Operating free-air temperature,		−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input Voltage				54			0.7	V
					74			0.8	
V_{IK}	Input clamp voltage		V_{CC}= Min, I_I=−18mA					−1.5	V
V_{OH}	High Level Output Voltage	MO	V_{CC}=Min, V_{IL}=Max	I_{OH}=−3mA		2.4			V
				I_{OH}=Max		2			
		D	V_{IH}=Min	I_{OH}=Max		2.4			
V_{OL}	Low Level Output Voltage	MO	V_{CC}=Min, V_{IH}=Min, V_{IL}=Max	I_{OL}=12mA	54, 74		0.25	0.4	V
				I_{OL}=24mA	74		0.35	0.5	
		D		I_{OL}=4mA	54,74		0.25	0.4	V
				I_{OL}=8mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied		V_{CC}=Max, V_O=2.7V. V_{IH}=Min, V_{IL}=Max					20	μA
I_{OZL}	Off-stage output current low-level voltage applied	MO	V_{CC}=Max, V_O=0.4V V_{IH}=Min, V_{IL}=Max					−20	μA
		D						−400	
I_I	**Input current at maximum input voltage**	D	V_{CC}=Max,	V_I=5.5V				100	μA
		All others		V_I=7V				100	
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	MO	V_{CC}=Max (Note 2)			−40		−225	mA
		D				−30		−130	
I_{CC}	Supply current		V_{CC}=Max	Outputs high			112	180	mA
				Outputs low			112	180	
				Output at high impedance			180	230	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Note more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS612 MIN	TYP	MAX	UNIT
t_{CSLDV}	Access (enable) time	$\overline{CS}$↓	D 0-11			26	50	ns
t_{WHDV}	Access (enable) time	R/$\overline{W}$↑	D 0-11	R_L = 2kΩ		20	35	ns
t_{RVDV}	Access time	RS	D 0-11	See Figure 1,		39	75	ns
t_{WLDZ}	Disable time	R/$\overline{W}$↓	D 0-11	See Note 2		30	50	ns
t_{CSHDZ}	Disable time	$\overline{CS}$↑	D 0-11			38	65	ns
t_{ELQV}	Access (enable) time	$\overline{ME}$↓	MO 0-11			17	30	ns
t_{CSHQV}	Access time	$\overline{CS}$↑	MO 0-11			48	85	ns
t_{MLQV}	Access time	$\overline{MM}$↓	MO 0-11	R_L = 667Ω		22	40	ns
t_{AVQV1}	Access time ($\overline{MM}$ low)	MA	MO 0-11	See Note 2		39	70	ns
t_{MHQV}	Access time	$\overline{MM}$↑	MO 0-11			22	40	ns
t_{AVQV2}	Propagation time ($\overline{MM}$ high)	MA	MO 8-11			13	30	ns
t_{EHQZ}	Disable time	$\overline{ME}$↑	MO 0-11			14	25	ns

Note 2: Access times are tested as t_{PLH} and t_{PHL} or t_{PZH} or t_{PZL}. Disable times are tested as t_{PHZ} and t_{PLZ}.

Explanation of Letter Symbols

This data sheet uses a new type of letter symbol to describe time intervals. The format is:

$$t_{AB\text{-}CD}$$

where: subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval.

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the sinals represented by A and C, respectively. One or two of the following is used:

- H= high or transition to high
- L= low or transition to low
- V= a valid steady-state level
- X= unknown, changing, or "don't care" level
- Z= high-impedance (off) state.

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur. For these letter symbols on this data sheet, the signal names are further abbreviated as follows:

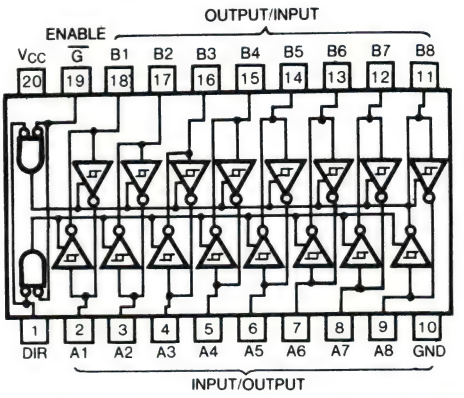
SIGNAL NAME	B or D SUBSCRIPT
C	C
$\overline{CS}$	CS
DO-11	D
MA0-MA3	A
MO0-MO11	Q
$\overline{ME}$	E
$\overline{MM}$	M
R/$\overline{W}$	W
RS0-RS3	R
$\overline{STROBE}$	S

GD54/74LS640, GD74LS640-1
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUT (INVERTED)

Features

- Inverting 3-STATE buffer outputs
- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- High Fan Out LS640: I_{OL}=24mA
  LS640-1: I_{OL}=48mA

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

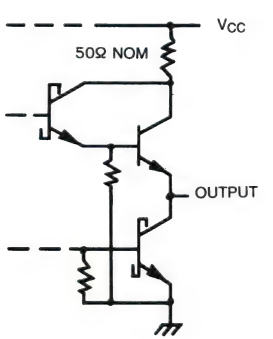
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data, from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

Function Table

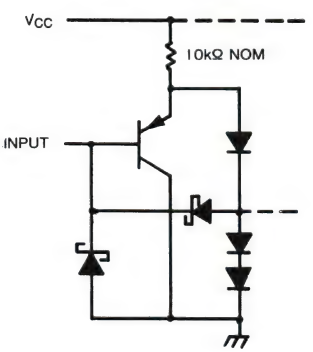
CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	LS640, LS640-1
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to b bus
H	X	Isolation

Schematics of Inputs and Outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF OUTPUTS



Recommended Operating Conditions

SYMBOL	PARAMETER		LS640			LS640-1			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	54	4.5	5	5.5				V
		74	4.75	5	5.25	4.75	5	5.25	
I_{OH}	High-level output current	54			−12				mA
		74			−15			−15	
I_{OL}	Low-level output current	54			12				mA
		74			24			48	
T_A	Operating free-air temperature	54	−55		125				°C
		74	0		70	0		70	

LS640

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.5	V
				74			0.6	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max	I_{OH}=−3mA		2.4	3.4		V
		I_{OH}=Max V_{IH}=Min	I_{OH}=Max		2			
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=12mA	54,74		0.25	0.4	V
			I_{OL}=24mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.7V, $\overline{G}$ at 2V					20	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.4V, $\overline{G}$ at 2V					−400	μA
I_I	Input current at maximum input voltage	V_{CC}=Max	V_I=5.5V	A or B			0.1	mA
			V_I=7V	DIR or $\overline{G}$			0.1	
I_{IH}	High-level input curent	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−40		−225	mA
I_{CC}	Total Supply Current	Outputs high	V_{CC}=Max, Outputs Open			48	70	mA
		Outputs low				62	90	
		Outputs at Z				64	95	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

LS640-1
Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.6	V
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IH}=Min, V_{IL}=Max	I_{OH}=−3mA	2.4	3.4		V
			I_{OH}=Max	2			
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=12mA		0.25	0.4	V
			I_{OL}=24mA		0.35	0.5	
			I_{OL}=48mA		0.4	0.5	
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.7V, $\overline{G}$ at 2V				20	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.4V, $\overline{G}$ at 2V				−400	μA
I_I	Input current at maximum input voltge	V_{CC}=Max, V_I=7V or V_I=5.5V				0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−225	mA
I_{CC}	Total Supply Current	Outputs high	V_{CC}=Max, Outputs, open		48	70	mA
		Outputs low			62	90	
		Outputs at Z			64	95	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS640, 'LS640—1 MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L=45pF, R_L=667Ω,		6	10	ns
		B	A			6	10	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			8	15	ns
		B	A			8	15	
t_{PZL}	Output enable time to low level	$\overline{G}$, DIR	A			31	40	ns
		$\overline{G}$, DIR	B			31	40	
t_{PZH}	Output enable time to high level	$\overline{G}$, DIR	A			23	40	ns
		$\overline{G}$, DIR	B			23	40	
t_{PLZ}	Output disable time from low level	$\overline{G}$, DIR	A	C_L=5pF, R_L=667Ω,		15	25	ns
		$\overline{G}$, DIR	B			15	25	
t_{PHZ}	Output disable time from high level	$\overline{G}$, DIR	A			15	25	ns
		$\overline{G}$, DIR	B			15	25	

TYPICAL CHARACTERISTICS

54LS'
INVERTING OUTPUT VOLTAGE
VS
INPUT VOLTAGE

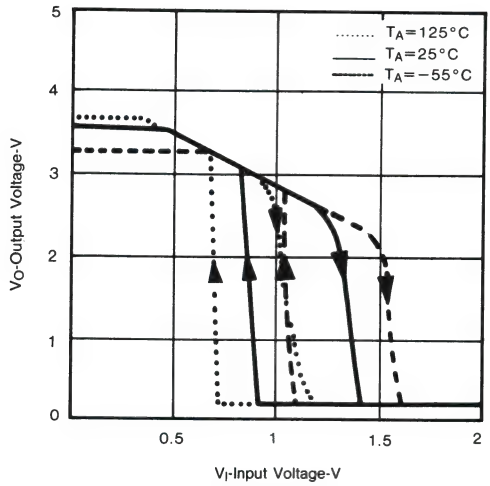


FIGURE 1

74LS'
INVERTING OUTPUT VOLTAGE
VS
INPUT VOLTAGE

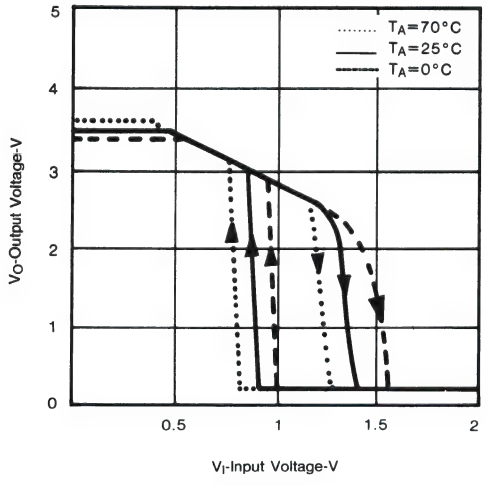


FIGURE 2

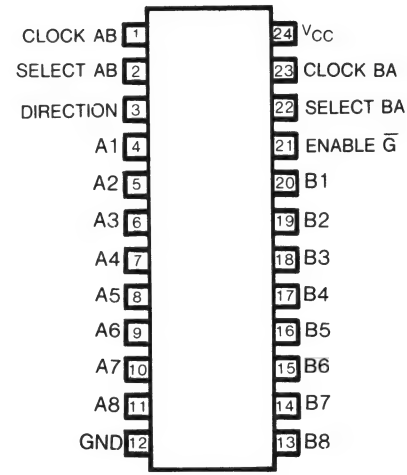
GD54/74LS646

OCTAL BUS TRANSCEIVERS AND REGISTERS

Features

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- 3-State Outputs

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

These devices consist of bus transceiver circuits with 3-state circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control $\overline{G}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled, and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

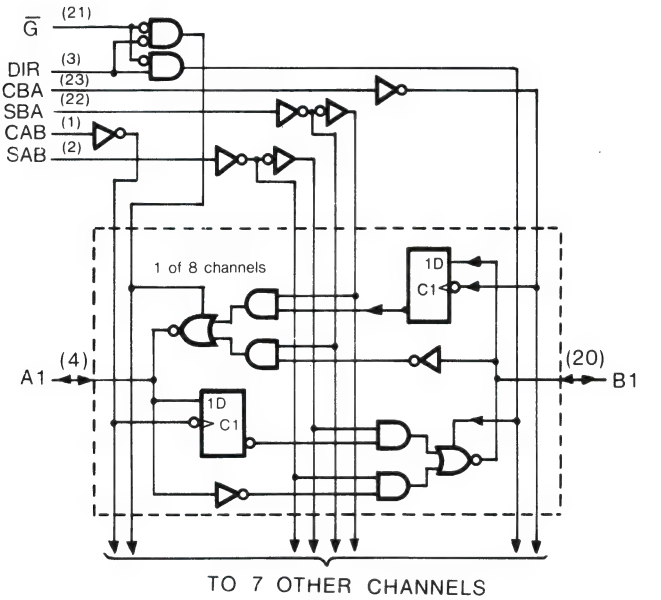
Function Table

INPUTS						DATA I/0		OPERATION OR FUNCTION
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'LS646
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

H=high level L=low level X=Irreievant ↑=low-to-high-level transition

- The date output function may be enabled or disabled by various signals at the $\overline{G}$ and DIR Inputs. Data input function are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

Function Block Diagram



Absolute Maximum Ratings at 25°C Free-air Temperature (Unless Otherwise Noted)

- Supply voltage, V_{CC} (see Note 1) 7V
- Input voltage (Control Inputs) 7V
- Off-state Output Voltage (A and B Ports) 5.5V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54			−12	mA
			74			−15	
I_{OL}	Low-level output current		54			12	mA
			74			24	
t_w	Width of any input pulse			20			ns
t_{su}	Clear inactive-state set up time	Bus to clock		20			ns
t_{th}	Data hold time	Bus from clock		0			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.5	V
				74			0.6	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18 mA					−1.5	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC}=Min,		54	0.1	0.4		V
				74	0.2	0.4		
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IH}=Min	I_{OH}=−3mA	54,74	2.4	3.4		V
		V_{IL}=Max	I_{OH}=Max	54,74	2			
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=12mA	54,74		0.25	0.4	V
			I_{OL}=24mA	74		0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.7V					−20	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.4V					−400	μA
I_I	Input current at maximum input voltage: A or B	V_{CC}=Max, V_I=5.5V	V_I=5.5V				0.1	mA
	Input current at maximum input voltage: All others		V_I=7V				0.1	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−40		−255	mA
I_{CC}	Supply Current: Output high	V_{CC}=5.25V, Outputs open				91	145	mA
	Supply Current: Outputs low					103	165	
	Supply Current: Outputs at Hi-z					103	165	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C

Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS646 MIN	TYP	MAX	UNIT
t_{PLH}	Clock	Bus	R_L=667Ω, C_L=45pF,		15	25	ns
t_{PHL}					23	35	ns
t_{PLH}	Bus	Bus			12	18	ns
t_{PHL}					13	20	ns
t_{PLH}	Select, with bus input high†	Bus			26	40	ns
t_{PHL}					21	35	ns
t_{PLH}	Select, with bus input low†				33	50	ns
t_{PHL}					14	25	ns
t_{PZH}	Enable	Bus			33	55	ns
t_{PZL}					42	65	ns
t_{PZH}	Direction				28	45	ns
t_{PZL}					39	60	ns
t_{PHZ}	Enable	Bus	R_L=667Ω, C_L=5pF,		23	35	ns
t_{PLZ}					22	35	ns
t_{PHZ}	Direction				20	30	ns
t_{PLZ}					19	30	ns

† These parameters are messured with the internal output state of the storage register opposite to that of the bus input.

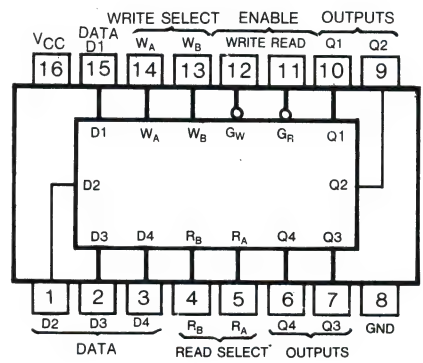
GD54/74LS670

TRI-STATE 4-by-4 REGISTER FILES

Features

- For use as:
  - Scratch pad memory
  - Buffer storage between processors
  - Bit storage in fast multiplication designs
- Separate read/write addressing permits simultaneous reading and writing
- Organized as 4 words of 4 bits
- Expandable to 512 words of n-bits

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

These register files are organized as 4 words of 4 bits each, and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits writing into one location, and reading from another word location, simultaneously.

Four data inputs are available to supply the word to be stored. Location of the word is determined by the write select inputs A and B, in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When, the write-enable input, $\overline{G}_W$, is high, the data will be accepted only if both internal address gate inputs are the information stored in the internal latches. When the read-enable input, $\overline{G}_R$, is high, the data outputs are inhibited and go into the high impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data entry addressing separate from data read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 ns typical) and the read time (24 ns typical). The register file has a non-volatile readout in that data is not lost when addressed.

All inputs (except read enable and write enable) are buffered to lower the drive requirements to one normal Series 54LS/74LS load, and input clamping diodes minimize switching transients to simplify system design. High speed, double ended ANO-OR-INVERT gates are employed for the read-address function and have high sink current. TRI-STATE outputs Up to 128 of these outputs may be wire-AND connected for increasing the capacity up to 5 12 words. Any number of these registers may be paralleled to provide n-bit word length.

Function Table

Write Table (See Notes A,B, and C)

Write Inputs			Word			
W_B	W_A	$\overline{G}_W$	0	1	2	3
L	L	L	Q = D	Q_O	Q_O	Q_O
L	H	L	Q_O	Q = D	Q_O	Q_O
H	L	L	Q_O	Q_O	Q = D	Q_O
H	H	L	Q_O	Q_O	Q_O	Q = D
X	X	H	Q_O	Q_O	Q_O	Q_O

Read Table (See Notes A and D)

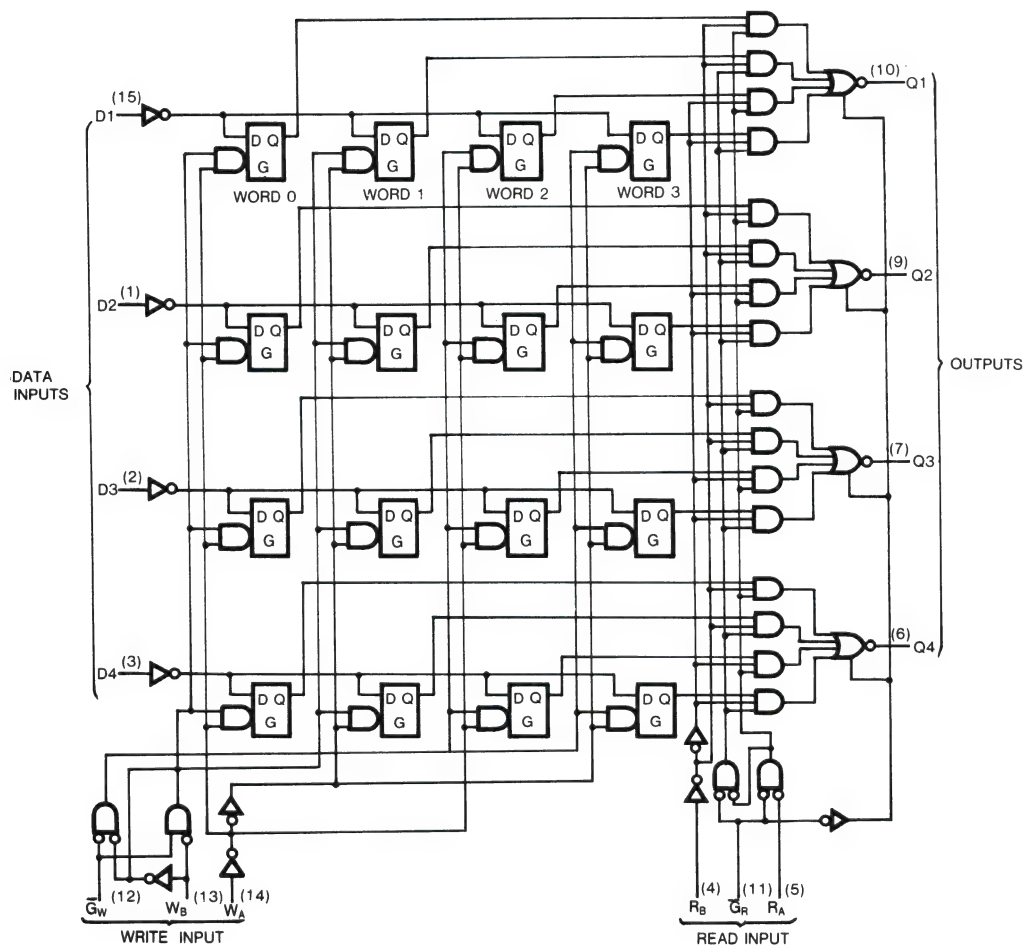
Read Inputs			Outputs			
R_B	R_A	$\overline{G}_R$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

Note A: H = High Level. L = Low Level. X = Don't Care.
Z = High Impedance (off)
Note B: (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs
Note C: Q_O = The level of Q before the indicated input conditions were established
Note D: WOB1 = The first bit of word O, etc.

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Off state output voltage 5.5V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Logic Diagram



Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54			−1	mA
			74			−2.6	
I_{OL}	Low-level output current		54			4	mA
			74			8	
t_W	Write Enable or Read Enable Pulse Width			25			ns
t_{SU}	Setup Time (Note 1)	Data		10			ns
		W_A,W_B		15			
t_H	Hold Time (Note 1)	Data		15			ns
		W_A,W_B		5			
t_{LATCH}	Latch Time for New Data(Note 2)			25			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Note 1: Times are with respect to the Write-Enable input. Write-Select time will protect the data written into the previous address. If protection of data in the previous address. $t_{SETUP}(W_AW_B)$ can be ignored. As any address selection sustained for the final 30 ns of the Write-Enable pulse and during $t_H(W_AW_B)$ will result in data being written into that location. Depending on the duration of the input conditions. one or a number of previous addresses may have been written into.

Note 2: Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempling to read from a location immediately after that location has received new data.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Read select	Any Q	C_L=15pF, R_L=2kΩ		23	40	ns
t_{PHL}			See Figures 1 and 2		25	45	
t_{PLH}	Write enable	Any Q			26	45	ns
t_{PHL}			C_L=15pF, R_L=2kΩ		28	50	
t_{PLH}	Data	Any Q	See Figures 1 and 3		25	45	ns
t_{PHL}					23	40	
t_{PZH}	Read enable	AnyQ	C_L=15pF, R_L=2kΩ		15	35	ns
t_{PZL}			See Figures 1 and 4		22	40	
t_{PHZ}			C_L=5pF, R_L=2kΩ		30	50	ns
t_{PLZ}			See Figures 1 and 4		16	35	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

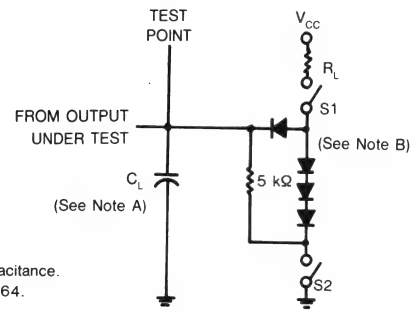
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I= −8mA					−1.5	V
V_{OH}	High level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.4	3.4		V
		I_{OH}=Max, V_{IH}=Min		74	2.4	3.1		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	D,R or W				0.1	mA
			$\overline{G}_W$				0.2	
			$\overline{G}_R$				0.3	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	D,R or W				20	μA
			$\overline{G}_W$				40	
			$\overline{G}_R$				60	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	D,R or W				−0.4	mA
			$\overline{G}_W$				−0.8	
			$\overline{G}_R$				−1.2	
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.7V, V_{IH}=Min					20	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.4V, V_{IH}=Min					−20	μA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−30		−130	mA
I_{CC}	Supply current	V_{CC}=Max(Note 3)				30	50	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C

Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Note 3: Maximum I_{CC} is guaranteed for the following worst case conditions: 4.5V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

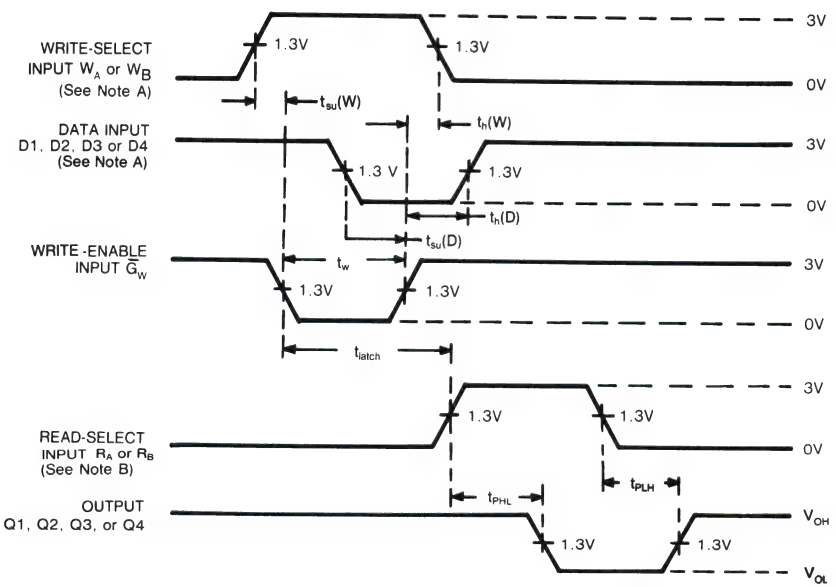
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.

LOAD CIRCUIT

FIGURE 1

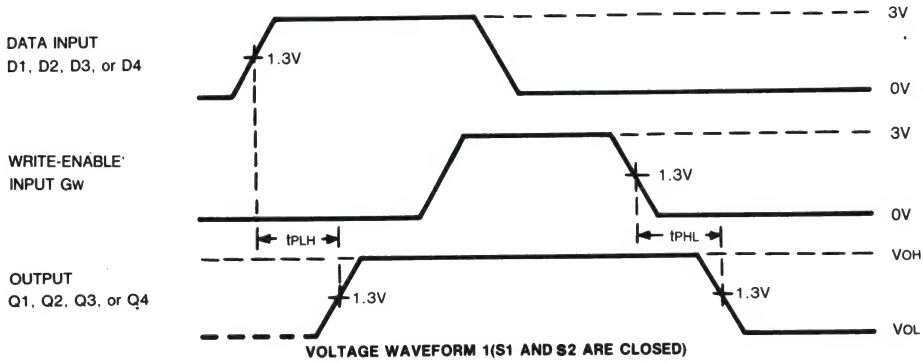


VOLTAGE WAVEFORMS (S1 AND S2 ARE CLOSED)

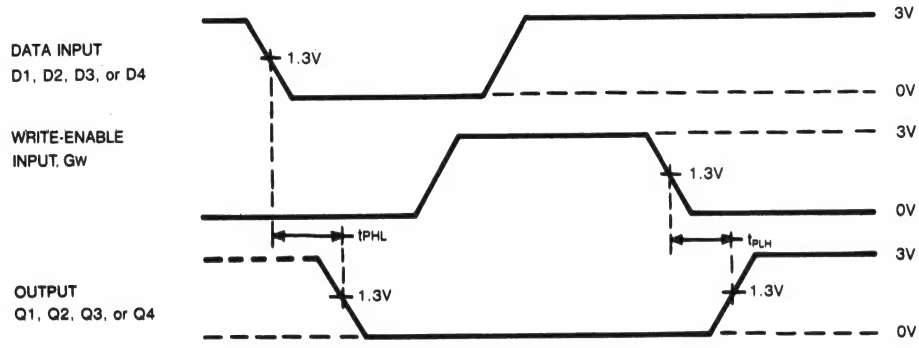
NOTES: A. High-level input pulses at the select and data inputs are illustrated however, times associated with low level pulses are measured from the same reference points.
B. When measuring delay times from a read select input, the read enable input is low.
C. Input waveforms are supplied by generators having the following characteristics: PRR ≤2 MHz. Zout ~ 50Ω, duty cycle ≤ 50%, t_r ≤ 15 ns, t_f ≤ 6 ns.

FIGURE 2

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM 1(S1 AND S2 ARE CLOSED)

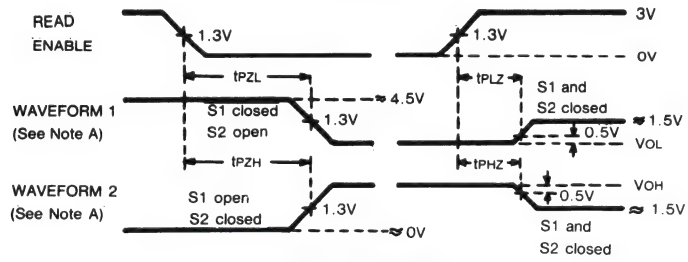


VOLTAGE WAVEFORM 2 (S1 AND S2 ARE CLOSED)

NOTES: A. Each select address is tested. Prior to the start of each of the above tests both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$ During the test G_R is low.

B. Input waveforms are supplied by generators having the following characteristics PRR $\leq$ 1 MHz, Zout $\sim$ 50Ω duty cycle $\leq$50%, $t_r \leq$ 15 ns, $t_f \leq$ 6 ns.

FIGURE 3



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. Waveforms 1 is for an output with internal conditions such that the output is low except when disabled by the read enable input. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the read enable input.

B. When measuring delay times from the read enable input, both read select inputs have been established at steady states.

C. Input waveforms are supplied by generators having the following characteristics: PRR $\leq$ 1MHz, Zout $\sim$ 50Ω duty cycle $\leq$50%, $t_r \leq$ 15 ns, $t_f \leq$ 6 ns.

FIGURE 4

GD54/74LS688

8-BIT MAGNITUDE COMPARATORS WITH TOTEM-POLE OUTPUTS

Feature

- Compares two 8 bit words
- Totem pole outputs
- Hysteresis is at P and Q intputs

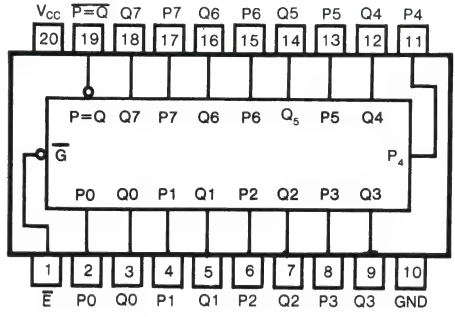
Description

The LS688 contanis 8 bit words comparator function with enable input.

When the enable input E is low, two eight bit binary or BCD words are applied at inputs P0∼P7 and Q0∼Q7.

The results are shown in function table.

Pin Configuration

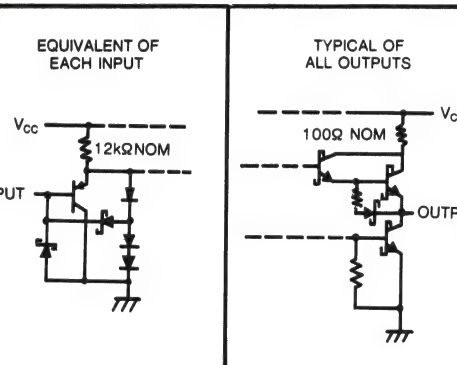


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

INPUTS		OUTPUT
P.Q	$\overline{E}$	$\overline{P=Q}$
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

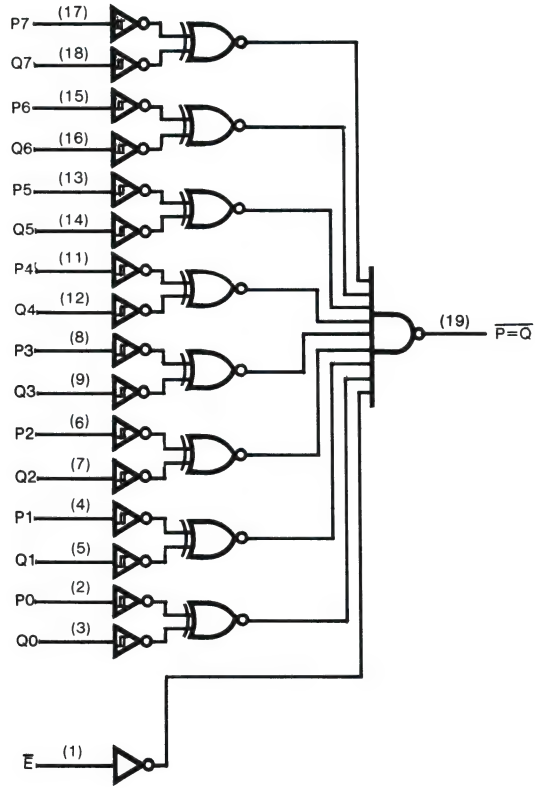
Schematics of Inputs and Outputs



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Function Block Diagram



Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER	FROM(INPUT)	TO(OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	P	$\overline{P=Q}$	$C_L=45pF$ $R_L=667\Omega$ all other inputs low state		12	18	ns
t_{PHL}					17	23	
t_{PLH}	Q	$\overline{P=Q}$			12	18	ns
t_{PHL}					17	23	
t_{PLH}	$\overline{E}$	$\overline{P=Q}$			12	18	ns
t_{PHL}					13	20	

For load circuit and voltage waveforms, see page 3-11.

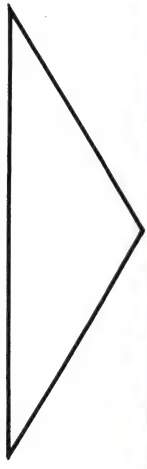
Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−400	μA
		74			−400	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC}=Min			0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IH}=Min		54	2.5	3.4		V
		V_{IL}=Max, I_{OH}=Max,		74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=12mA	54,74		0.25	0.4	V
			I_{OL}=24mA	54		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max,	V_I=5.5V Q inputs				0.1	mA
			V_I=7V other inputs				0.1	
I_{IH}	HIgh-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max,	V_I=0.4V Q inputs				−0.4	mA
			V_I=0.4V other inputs				−0.2	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V, (Note 3)				40	65	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with any $\overline{E}$ inputs grounded, all other inputs at 4.5V, and all outputs open.



NUMERICAL/FUNCTIONAL INDEX 1

FUNCTIONAL INDEX/SELECTION GUIDE 2

TTL CHARACTERISTICS 3

GD74LS FAMILY CIRCUITS 4

GD74S FAMILY CIRCUITS 5

QUALITY ASSURANCE MANUAL 6

ORDERING INFORMATION & PACKAGE DIMENSION 7

GOLDSTAR SEMICONDUCTOR SALES NETWORK 8

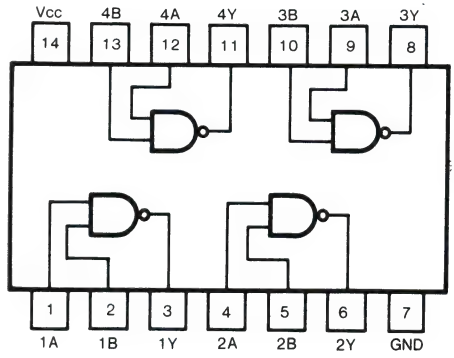
GD54/74S00

QUADRUPLE 2-INPUT POSITIVE NAND GATES

Description

This device contains four independent 2-input NAND gates. It performs the Boolean functions $Y=\overline{A \cdot B}$ or $Y=\overline{A}+\overline{B}$ in positive logic.

Pin Configuration

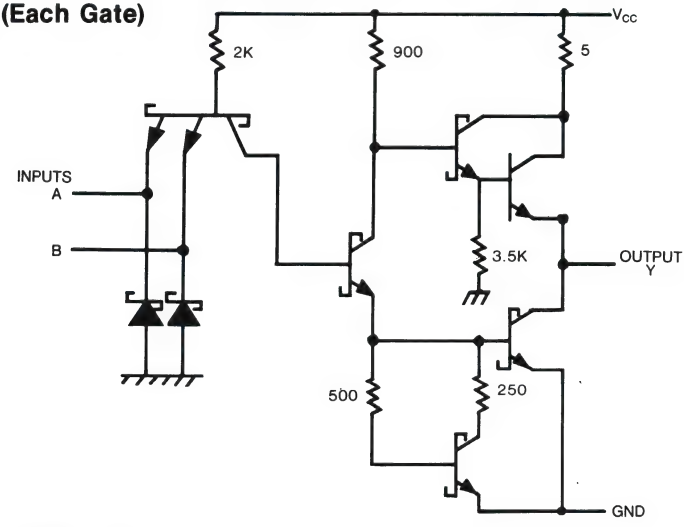


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

Schematics (Each Gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 5.5V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.8	V
				74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC}=Min, V_{IL}=Max, I_{OH}=Max	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC}=Min, I_{OL}=Max, V_{IH}=Min				0.5	V
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)		−40		−100	mA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max			10	16	mA
I_{CCL}		Toal with outputs low	V_{CC}=Max			20	36	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=280Ω		3	4.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3	5	

#For load circuit and voltage waveforms, see page 3-12.

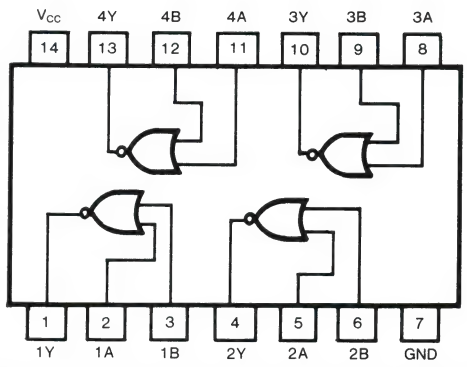
GD54/74S02

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

Description

This device contains four independent 2-input NOR gates. It performs the Boolean functions $Y=\overline{A}\cdot\overline{B}$ or $Y=\overline{A+B}$ in positive logic.

Pin Configuration

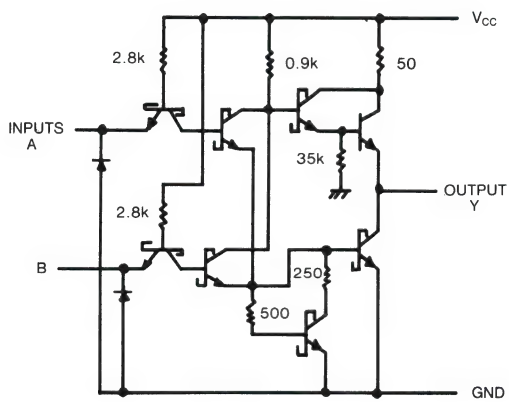


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

Circuit Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S .....−55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54, 74			−1	mA
I_{OL}	Low-level output current	54, 74			20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max,	54	2.5	3.4		V
			74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, I_{OL}=Max, V_{IH}=Min				0.5	V
I_I	Input current at maximun input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max			17	29	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max			26	45	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=280Ω		3.5	5.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3.5	5.5	

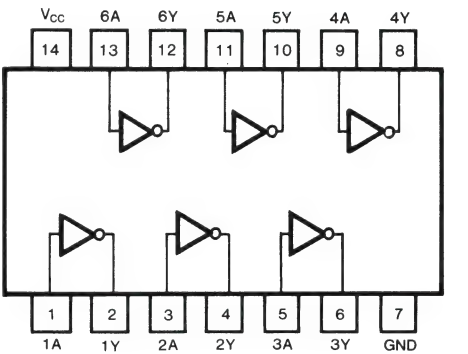
#For load circuit and voltage waveforms, see page 3-12.

GD54/74S04
HEX INVERTERS

Description

This device contains six independent inverters. It performs the Boolean function $Y=\overline{A}$.

Pin Configuration

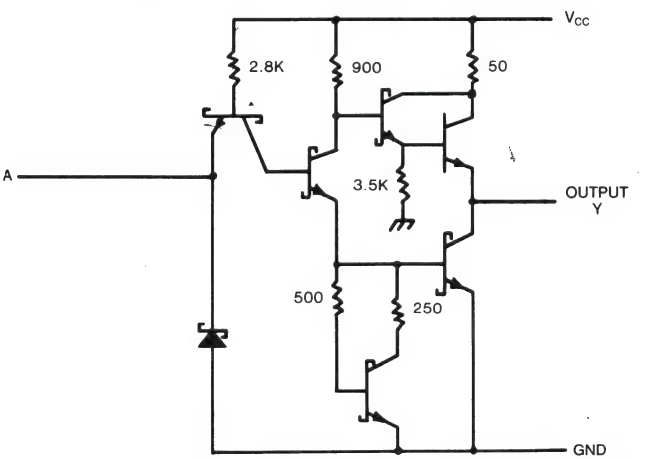


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

Schematics (each inverter)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.8	V
				74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC}=Min, V_{IL}=Max, I_{OH}=Max	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC}=Min, I_{OL}=Max, V_{IH}=Min				0.5	V
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)		−40		−100	mA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max			15	24	mA
I_{CCL}		Toal with outputs low	V_{CC}=Max			30	54	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=280Ω		3	4.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3	5	

#For load circuit and voltage waveforms, see page 3-12.

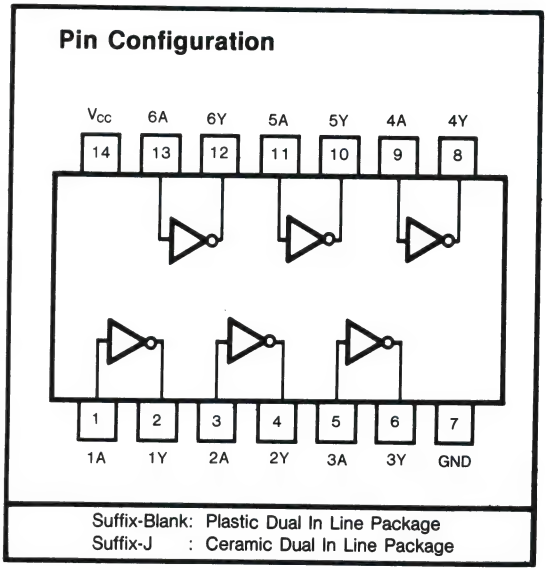
GD54/74S05

HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

Description

This device contains six independent inverters. It performs the Boolean function $Y=\overline{A}$. The open collector outputs require pull-up resistor to perform correctly. Open-collector devices are often used to generate higher V_{OH} levels.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

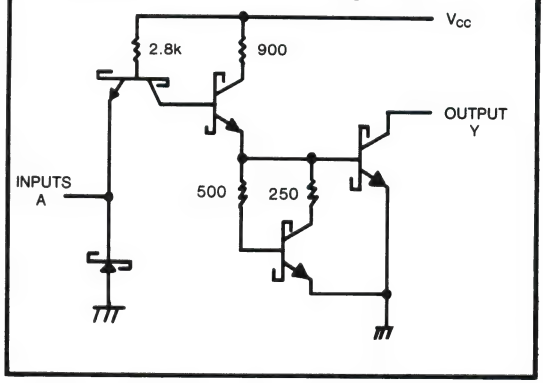
Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}(Min) - V_{OH}}{N_1(I_{OH}) + N_2(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}(Max) - V_{OL}}{I_{OL} - N_3(I_{IL})}$$

Where: N_1 (I_{OH})=total maximum output high current for all outputs tied to pull-up resistor
N_2 (I_{IH})=total maximum input high current for all inputs tied to pull-up resistor
N_3(I_{IL})=total maximum input low current for all inputs tied to pull-up resistor

Circuit Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
V_{OH}	High-level output voltage	54, 74			5.5	V
I_{OL}	Low-level output current	54, 74			20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA			−1.2	V
I_{OH}	High-level output current		V_{CC}=Min, V_{OH}=Max, V_{IL}=Max			250	μA
V_{OL}	Low-level output voltage		V_{CC}=Min I_{OL}=Max, V_{IH}=Min			0.5	V
I_I	Input current at maximun input voltage		V_{CC}=Max, V_I=5.5V			1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V			50	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.5V			−2	mA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max		9.0	19.8	mA
I_{CCL}		Total with outputs low	V_{CC}=Max		30	54	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time low-to-high-level output	C_L=15pF, R_L=280Ω		5	7.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			4.5	7	

#For load circuit and voltage waveforms, see page 3-12.

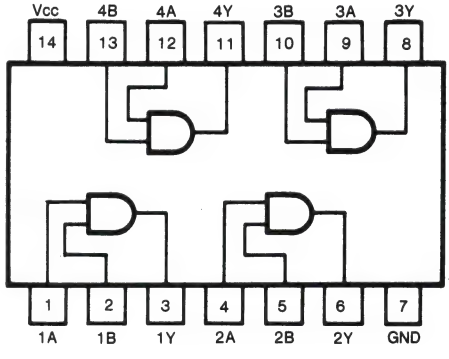
GD54/74S08

QUADRUPLE 2-INPUT POSITIVE AND GATES

Description

This device contains four independent 2-input AND gates. It performs the Boolean functions $Y=A \bullet B$ or $Y=\overline{\overline{A}+\overline{B}}$ in positive logic.

Pin Configuration

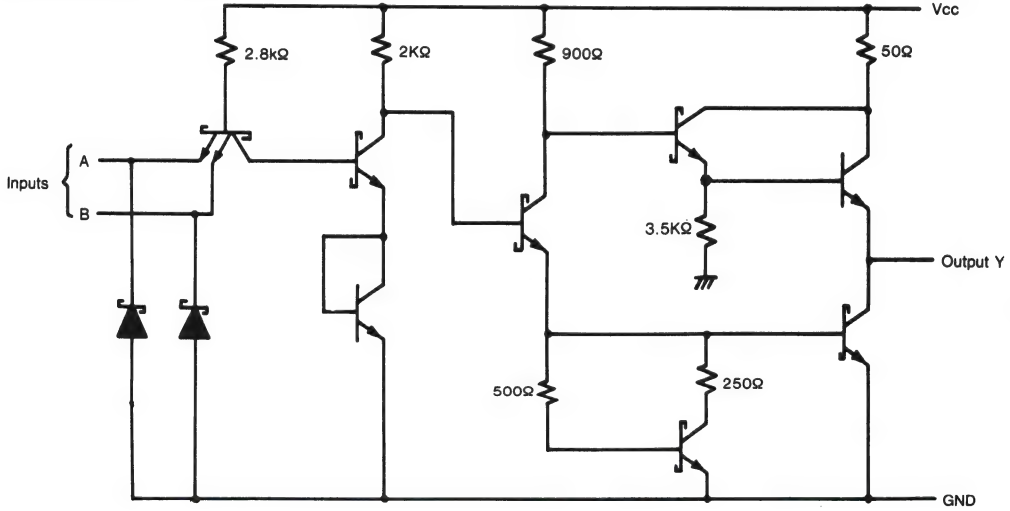


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table(each gate)

INPUT		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

Circuit Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 5.5V
- Operating free-air temperature range 54 S ..... −65°C to 150°C
  74 S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1000	μA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18 mA				−1.2	V
V_{OH}	High level output voltage	V_{CC}=Min, I_{OH}=Max, V_{IH}=Min	54	2.5	3.4		V
			74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OL}=Max,				0.5	V
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max		18	32	mA
I_{CCL}		Total with outputs low	V_{CC}=Max		32	57	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=280Ω		4.5	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output			5	7.5	

#For load circuit and voltage waveforms, see page 3-12.

GD54/74S10

TRIPLE 3-INPUT POSITIVE NAND GATES

Description

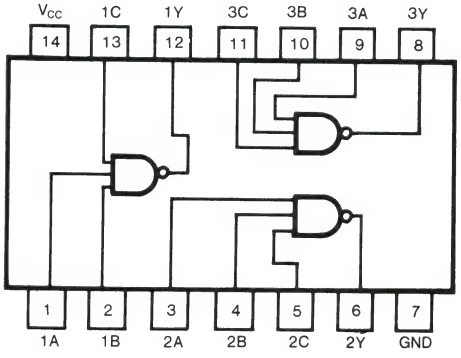
This device contains three independent 2-input NAND gates. It performs the Boolean functions $Y=\overline{A \cdot B \cdot C}$ or $Y=\overline{A}+\overline{B}+\overline{C}$ in positive logic.

Function Table (each gate)

INPUTS		OUTPUT
A	N*	Y
L	L	H
H	L	H
L	H	H
H	H	L

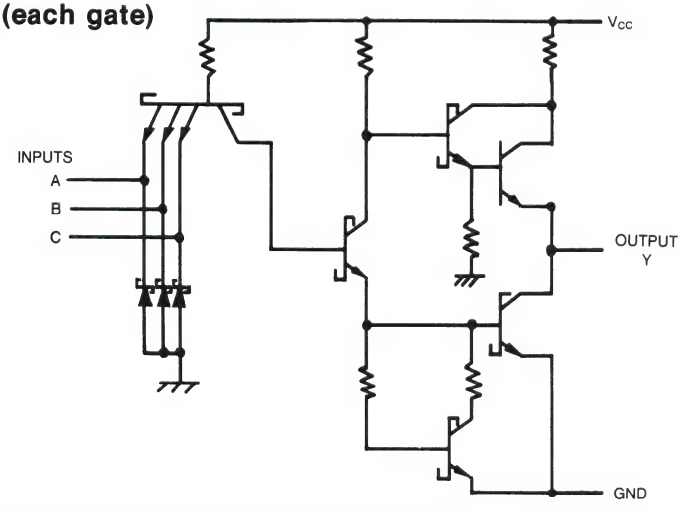
* N=B·C

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max, V_{IH}=Min	54	2.5	3.4		V
			74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, I_{OL}=Max, V_{IH}=Min				0.5	V
I_I	Input current at maximun input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max			7.5	12	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max			15	27	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=280Ω		3	4.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3	5	

#For load circuit and voltage waveforms, see page 3-12.

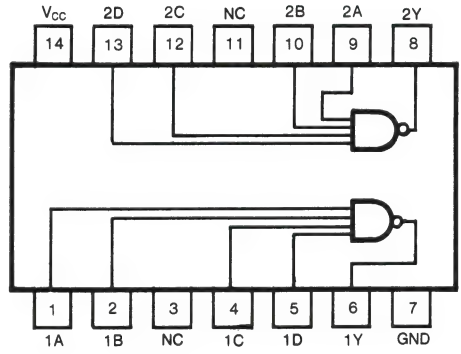
GD54/74S20

DUAL 4-INPUT POSITIVE NAND GATES

Description

This device contains two independent 4-input NAND gates. It performs the Boolean functions, $Y=\overline{A.B.C.D}$ or $Y=\overline{A}+\overline{B}+\overline{C}+\overline{D}$ in positive logic.

Pin Configuration



NC: No internal connection

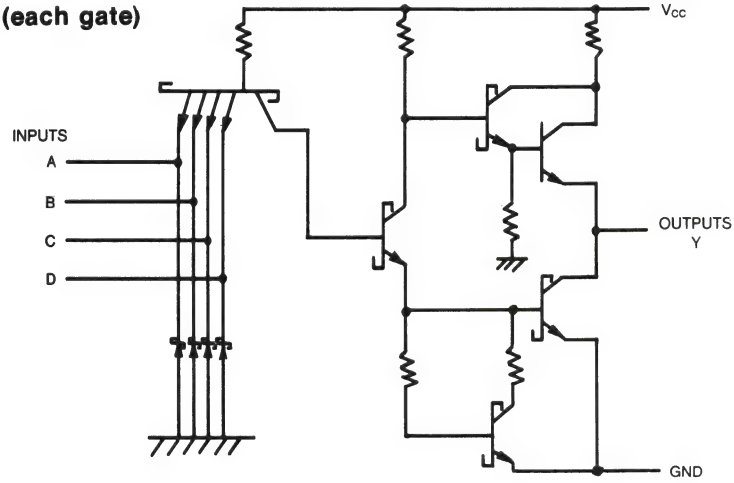
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each gate)

INPUTS		OUTPUT
A	N*	Y
L	L	H
H	L	H
L	H	H
H	H	L

*N=B·C·D

Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S .....−55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max	54	2.5	3.4		V
			74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IH}=Min, I_{OL}=Max				0.5	V
I_I	Input current at maximun input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CCH}	Supply current, Total with outputs high	V_{CC}=Max			5	8	mA
I_{CCL}	Supply current, Total with outputs low	V_{CC}=Max			10	18	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=280Ω		3	4.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3	5	

#For load circuit and voltage waveforms, see page 3-12.

GD54/74S30

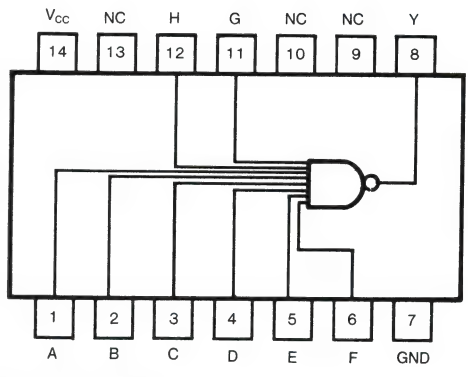
8-INPUT POSITIVE NAND GATE

Description

This device contains a single 4-input NAND gate and performs the following Boolean functions in positive logic.

$$Y=\overline{A.B.C.D.E.F.G.H} \text{ or}$$
$$Y=\overline{A}+\overline{B}+\overline{C}+\overline{D}+\overline{E}+\overline{F}+\overline{G}+\overline{H}$$

Pin Configuration



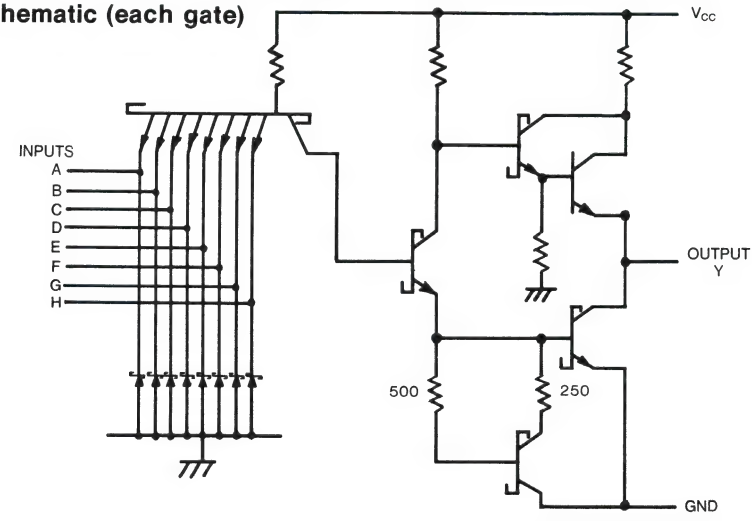
NC: No internal connection

Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

Circuit Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S .....−55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	Typ (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.8	V
				74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC}=Min, V_{IL}=Max, I_{OH}=Max	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC}=Min, V_{IH}=Min, I_{OL}=Max				0.5	V
I_I	Input current at maximun input voltage		V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)		−40		−100	mA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max			3	5	mA
I_{CCL}		Total with outputs low	V_{CC}=Max			5.5	10	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=280Ω		4	6	ns
t_{PHL}	Propagation delay time, high-to-low-level output			4.5	7	

#For load circuit and voltage waveforms, see page 3-12.

GD54/74S32

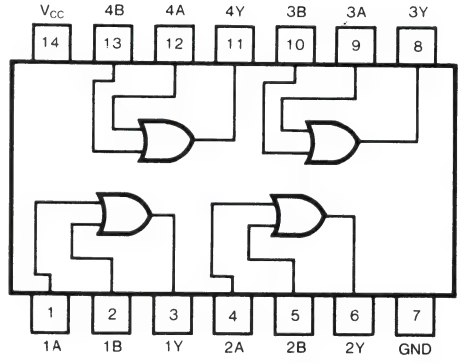
QUADRUPLE 2-INPUT POSITIVE OR GATES

Description

The use of schottky TTL technology has enabled the achievement of high input/output voltages and high speed.

This device contains four independent 2-input OR gates. It performs the Boolean functions $Y=\overline{\overline{A}\cdot\overline{B}}$ or $Y=A+B$ in positive logic.

Pin Configuration

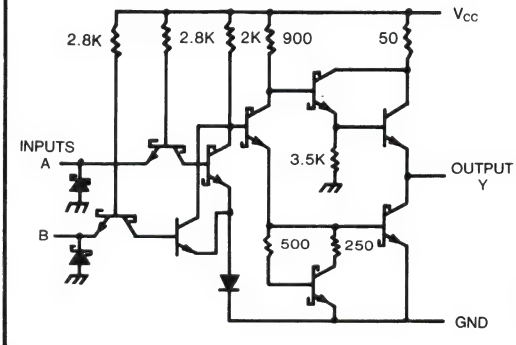


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (Each Gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

Circuit Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.8	V
				74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC}=Min, V_{IH}=Min, I_{OH}=Max	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC}=Min, V_{IL}=Max, I_{OL}=Max				0.5	V
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)		−40		−100	mA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max			18	32	mA
I_{CCL}		Total with outputs low	V_{CC}=Max			38	68	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=280Ω		4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output			4	7	

#For load circuit and voltage waveforms, see page 3-12.

GD54/74S51

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

Description

This device contains two independent combinations of gates each of which performs the logic AND-OR-INVERT function.

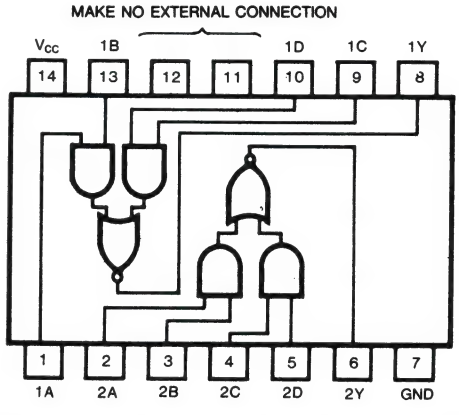
$$Y=\overline{AB+CD}$$

Function Table

Inputs				Output
A	B	C	D	Y
H	H	X	X	L
X	X	H	H	L
All other combinations				H

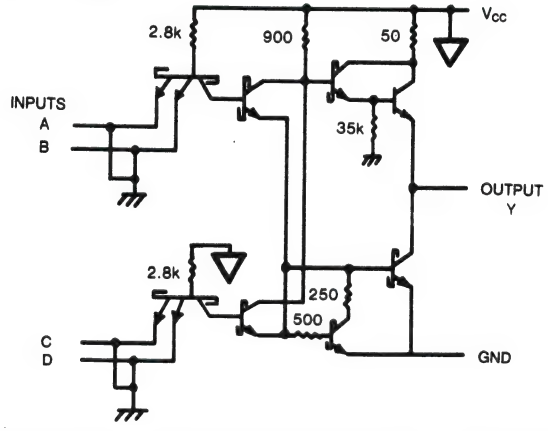
H=High Logic Level
L=Low Logic Level
X=Irrelevant

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Circuit Schematic (each gate)



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S .....−55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.8	V
				74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC}=Min, V_{IL}=Max, I_{OH}=Max,	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC}=Min, V_{IH}=Min, I_{OL}=Max,				0.5	V
I_I	Input current at maximun input voltage		V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V				20	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)		−40		−100	mA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max			8.2	17.8	mA
I_{CCL}		Total with outputs low	V_{CC}=Max			14	22	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=280Ω		3.5	5.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3.5	5.5	

#For load circuit and voltage waveforms, see page 3-12.

GD54/74S64

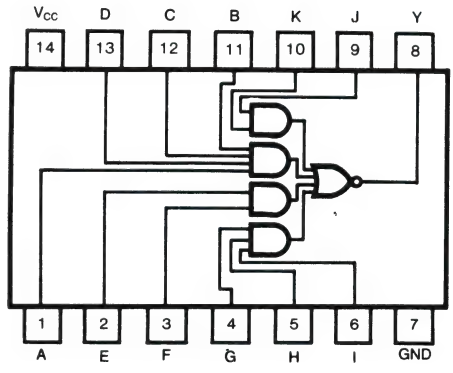
4-WIDE AND-OR-INVERT GATES

Description

This device contains two independent combinations of gates each of which performs the logic AND-OR-INVERT function.

$Y=\overline{ABCD+EF+GHI+JK}$

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

Inputs											Output
A	B	C	D	E	F	G	H	I	J	K	Y
H	H	H	H	X	X	X	X	X	X	X	L
X	X	X	X	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

H=High Logic Level
L=Low Logic Level
X=Either Low or High Logic Level

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55° to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max	54	2.5	3.4		V
			74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IH}=Min, I_{OL}=Max				0.5	V
I_I	Input current at maximun input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max		7	12.5	mA
I_{CCL}		Total with outputs low	V_{CC}=Max		8.5	16	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=280Ω		3.5	5.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3.5	5.5	

#For load circuit and voltage waveforms, see page 3-12.

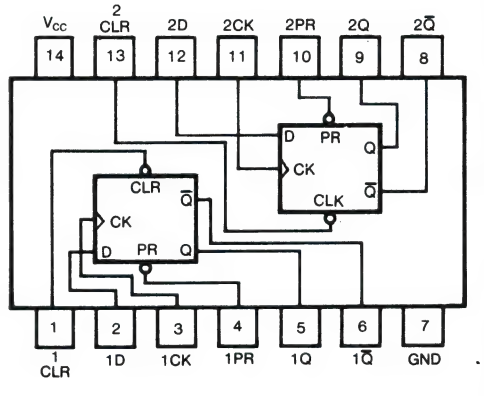
GD54/74S74

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

Description

This device contains two independent D-type positive edge triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

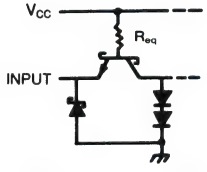
Function Table (each flip-flop)

OUTPUTS		INPUTS		
Q	Q↑	CLEAR	CLOCK	D
L	H	L	X	X
H	L	H	↑*	H
L	H	H	↑*	L
Q_0	Q_0	H	L	X

* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum, Furthermore, this configuration is nonstable; that is it will not persist when either preset or clear returns to its inactive (high) level.

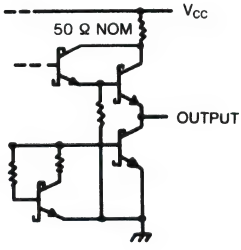
Schematics of Inputs and Outputs

EQUIVALENT OF EACH INPUT

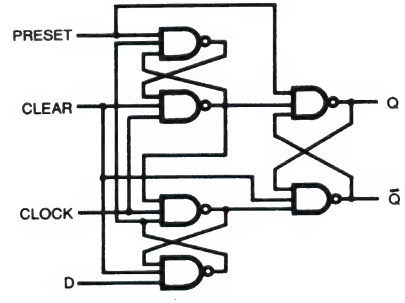


I_{IL} MAX	R_{eq} NOM
− 1.6 mA	4 kΩ
− 2 mA	2.8 kΩ
− 4 mA	1.4 kΩ
− 6 mA	940 Ω
− 7 mA	900 Ω
− 8 mA	700 Ω
− 14 mA	450 Ω

TYPICAL OF ALL OUTPUTS



Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- output voltage 7V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current					−1	mA
I_{OL}	Low-level output current					20	mA
t_w	Pulse width	clock high		6			ns
		clock low		7.3			
		clear or preset low		7			
t_{SU}	Input setup time	High-level data		3↑			ns
		Low-level data		3↑			
t_h	Input hold time			2↑			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

↑ For rising edge

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.8	V
				74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC}=Min V_{IL}=Max I_{OH}=Max V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC}=Min V_{IL}=Max I_{OL}=Max V_{IH}=Min				0.5	V
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	J, K or D	V_{CC}=Max V_I=2.7V				50	μA
		Clear					150	
		Preset					100	
		Clock					100	
I_{IL}	Low-level input current	J, K or D	V_{CC}=Max V_I=0.5V				−2	mA
		Clear*					−6	
		Preset*					−4	
		Clock					−4	
I_{OS}	Short-circuit output current		V_{CC}=Max		−40		−100	mA
I_{CC}	Supply current (average per F/F)		V_{CC}=Max (Note 3)			15	25	mA

Note 1: All typial values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}			$C_L=15pF$ $R_L=280\Omega$	75	110		MHz
t_{PLH}	Preset or clear	Q or $\overline{Q}$			4	6	ns
t_{PHL}	Preset or clear (clock high)	$\overline{Q}$ or Q			9	13.5	ns
	Preset or clear (clock low)				5	8	
t_{PLH}	Clock	Q or $\overline{Q}$			6	9	ns
t_{PHL}					6	9	

* f_{max}=maximum clock frequency
t_{PLH}=propagation delay time, low-to-high-level output.
t_{PHL}=propagation delay time, high-to-low-level output.
#For load circuit and voltage waveforms, see page 3-12.

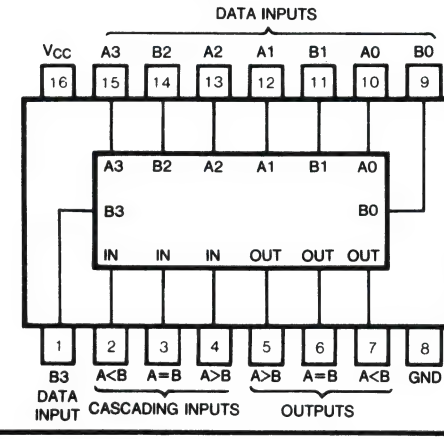
GD54/74S85

4-BIT MAGNITUDE COMPARATORS

Description

These four-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two, 4-bit words (A,B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A>B, A<B, and A=B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A=B input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

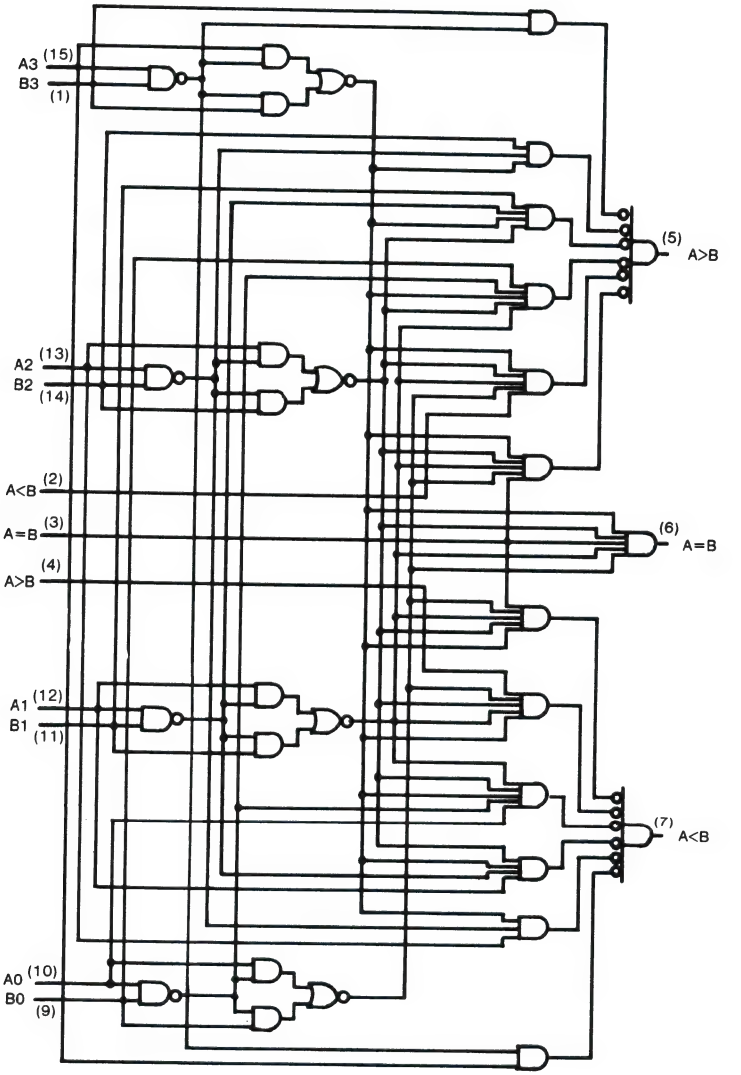
Comparing				Cascading Inputs			Outputs		
A3,B3	A2,B2	A1,B1	A0,B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

H=High Level, L=Low Level, X=Don't Care

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Function Block Diagram



Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.55	5	5.25	
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	Typ (Note 1)	MAX	UNIT
V_{IH}	High level input voltage				2			V
V_{IL}	Low level input voltage			54			0.8	V
				74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High level output voltge		V_{CC}=Min, V_{IL}=Max	54	2.5	3.4		V
			I_{OH}=Max, V_{IH}=Min	74	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC}=Min, V_{IL}=Max I_{OL}=Max, V_{IH}=Min				0.5	V
I_I	Input current at maximum input voltage		V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	A<B, A>B inputs	V_{CC}=Max, V_I=2.7V				50	μA
		all other inputs					150	
I_{IL}	Low-level input current	A<B, A>B inputs	V_{CC}=Max, V_I=0.5V				−2	mA
		all other inputs					−6	
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)		−40		−100	mA
I_{CC}	Supply current		V_{CC}=Max (Note 3)			73	115	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with outputs open, A=B grounded, and all other inputs at 4.5V.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A<B, A>B	1	$C_L=15pF$, $R_L=280\Omega$,		5		ns
			2			7.5		
			3			10.5	16	
		A=B	4			12	18	
t_{PHL}	Any A or B data input	A<B, A>B	1			5.5		ns
			2			7		
			3			11	16.5	
		A=B	4			11	16.5	
t_{PLH}	A<B or A=B	A>B	1			5	7.5	ns
t_{PHL}	A<B or A=B	A>B	1			5.5	8.5	ns
t_{PLH}	A=B	A=B	2			7	10.5	ns
t_{PHL}	A=B	A=B	2			5	7.5	ns
t_{PLH}	A>B or A=B	A<B	1			5	7.5	ns
t_{PHL}	A>B or A=B	A<B	1			5.5	8.5	ns

t_{PLH} = propagation delay time, low to high level output
t_{PHL} = propagation delay time, high to low level output

APPLICATIONS—Figure A shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure b six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table 1.

TABLE 1

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2-6
25-120 Bits	8-31

NOTE:
The 54/74S85 can be used as a 5-bit comparator only when the outputs are used to drive the A_0-A_3 and B_0-B_3 inputs of another 54/74LS as shown in Figure B in positions #1,2,3, and 4.

MSB=Most Significant Bit
LSB=Least Significant Bit
L=LOW Level
H=HIGH Level
NC=No Connection

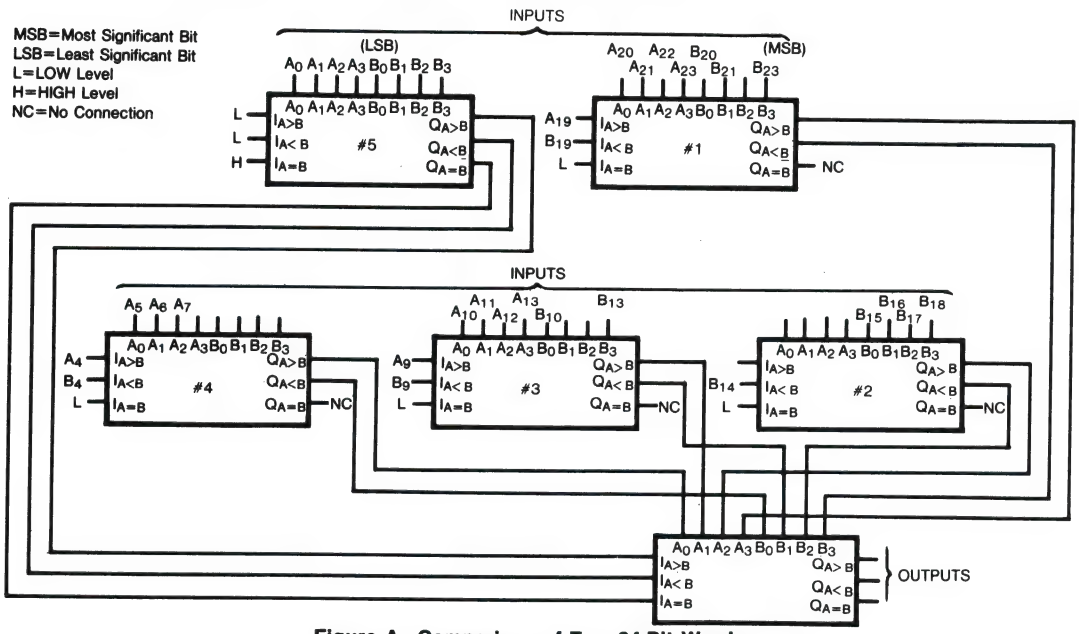


Figure A. Comparison of Two 24-Bit Words

GD54/74S86

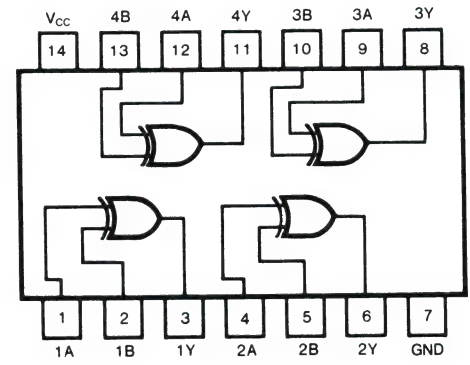
QUADRUPLE 2-INPUT EXCULSIVE-OR GATES

Description

This device contains four independent 2-input Exclusive-OR gates. It performs the Boolean functions $Y=A \oplus B=\bar{A}B+A\bar{B}$ inpositive logic.

When both inputs A and B either low or high, output Y is low, and when A and B are high and low and low and high respectively, Y is high.

Pin Configuration

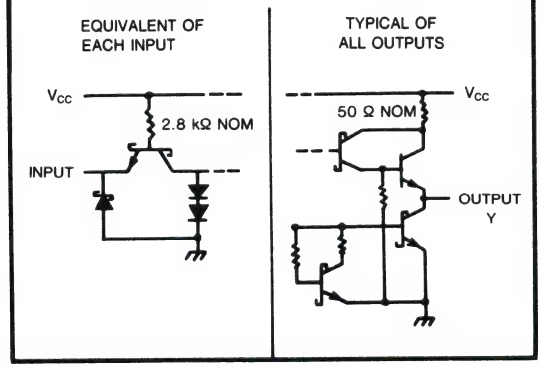


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Schematics of Inputs and Outputs



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min V_{IL}=Max I_{OH}=Max V_{IH}=Min	54	2.5	3.4		V
			74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max I_{OL}=Max V_{IH}=Min				0.5	V
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V, See Note 3			50	75	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
Note 3: I_{CC} is measured with the inputs grounded and outputs open.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

PARAMETER*	FROM (INPUT)	TEST CONDITION#		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L=15pF R_L=280Ω		7	10.5	ns
t_{PHL}					6.5	10	
t_{PLH}	A or B	Other input high			7	10.5	ns
t_{PHL}					6.5	10	

* t_{PLH}=propagation delay time, low-to-high-level output
t_{PHL}=propagation delay time, high-to-low-level output
#For load circuit and voltage waveforms, see page 3-12.

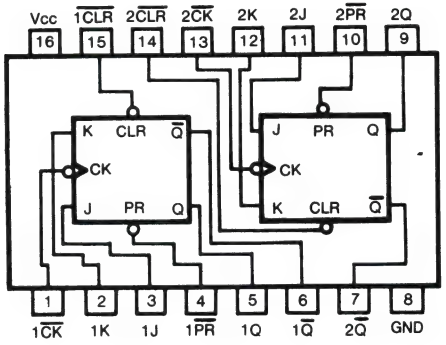
GD54/74 S112

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH SET AND RESET

Features

- Negative edge-triggering
- Independent input/output terminals for each flip-flop.
- Direct set and reset inputs
- Q and $\overline{Q}$ outputs

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

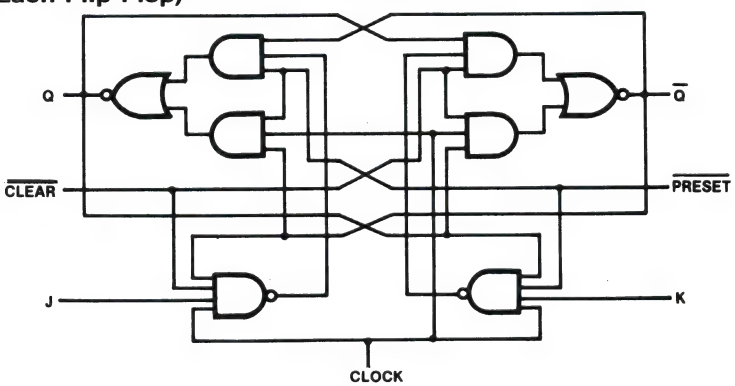
This device contains two independent negative-edgetriggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs can be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Function Table

Inputs					Outputs	
$\overline{PR}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_o	$\overline{Q}_o$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_o	$\overline{Q}_o$

↓=Negative Going Edge Pulse
•=This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive(high) level.
Q_o=The output logic level before the indicated input conditions were established.
Toggle=Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Block Diagram (Each Flip Flop)



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 5.5V
- Operating free-air temperature range 54 S..... −55°C to 125°C
  74 S..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current					−1	mA
I_{OL}	Low-level output current					20	mA
tw	Pulse width	clock high		6			ns
		clock low		6.5			
		clear or preset low		8			
t_{SU}	Input setup time	High-level data		3↓			ns
		Low-level data		3↓			
t_h	Input hold time			0↓			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

PARAMETER*	FROM(INPUT)	TO(OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}			C_L=15pF, R_L=280Ω	80	125		MHz
t_{PLH}	Preset or clear	Q or $\overline{Q}$			4	7	ns
t_{PHL}	Preset or clear (clock high)	Q or $\overline{Q}$			5	7	ns
	Preset or clear (clock low)	$\overline{Q}$ or Q			5	7	
t_{PLH}	Clock	Q or $\overline{Q}$			4	7	ns
t_{PHL}					5	7	

*f_{max}= maximum clock frequency
t_{PLH}= propagation delay time, low-to-high-level output.
t_{PHL}= propagation delay time, high-to-low-level output.

#For load circuit and voltage waveforms, see page 3-12.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min	54	2.5	3.4		V
			74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OL}=Max, V_{IH}=Min				0.5	V
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	J,K			50	μA
			$\overline{\text{Clear}}$			100	
			$\overline{\text{Preset}}$			100	
			Clock			100	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V (Note 4)	J,K			−1.6	mA
			$\overline{\text{Clear}}$			−7	
			$\overline{\text{Preset}}$			−7	
			Clock			−4	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)			30	50	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted a time, and the duration should not exceed one second.
Note 3: With all output open, I_{CC} is measured with the Q and $\overline{Q}$ output high in turn. At the time of measurement, the clock input is grounded.
Note 4: Clear is tested with preset high and preset is tested with clear high.

GD54/74S133

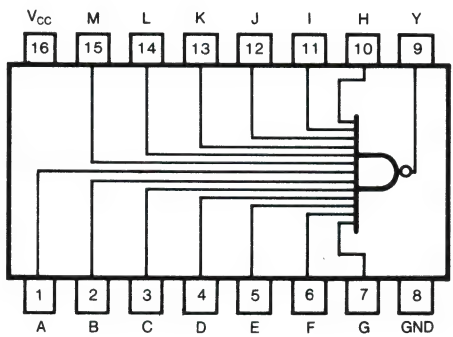
13-INPUT NAND GATE

Description

This device contains a single gate which performs the logic NAND function.

$Y=\overline{ABCDEFGHIJKLM}$

Pin Configuration



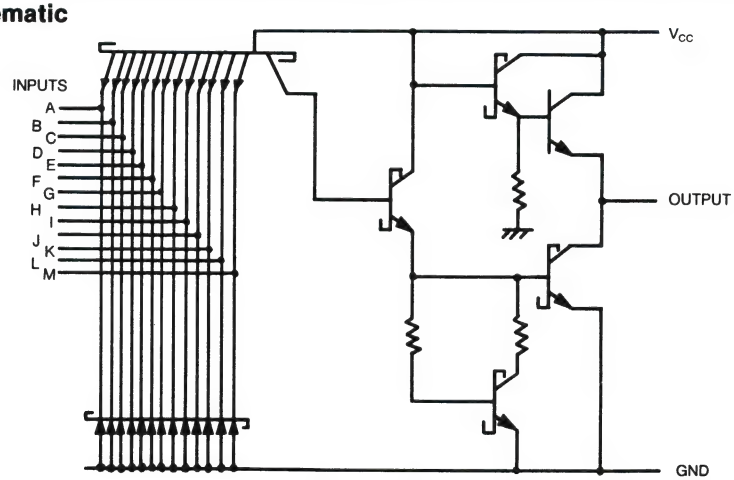
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

Inputs	Output
A thru M	Y
All Inputs H	L
One or More Input L	H

H=High Logic Level
L=Low Logic Level

Circuit Schematic



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S .....−55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54, 74			−1	mA
I_{OL}	Low-level output current	54, 74			20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.8	V
				74			0.8	
V_{IK}	Input clamp voltage		V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC}=Min, V_{IL}=Max, I_{OH}=Max	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC}=Min, I_{OL}=Max, V_{IH}=Min				0.5	V
I_I	Input current at maximun input voltage		V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current		V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current		V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current		V_{CC}=Max (Note 2)		−40		−100	mA
I_{CCH}	Supply current	Total with outputs high	V_{CC}=Max			3	5	mA
I_{CCL}		Total with outputs low	V_{CC}=Max			5.5	10	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L=15pF, R_L=280Ω			6	ns
t_{PHL}	Propagation delay time, high-to-low-level output			4.5	7	

#For load circuit and voltage waveforms, see page 3-12.

GD54/74S138

3-TO-8 LINE DECODERS/DEMULTIPLEXERS

Feature

- Designed Specifically for High Speed Memory Decodes and Data Transmission Systems
- Incorporate 3 Enable Inputs to Simplify Cascading and/or Data Rejection
- Contains Two Fully Independent 2-to-4 Line Decoders/ Demultiplexers.

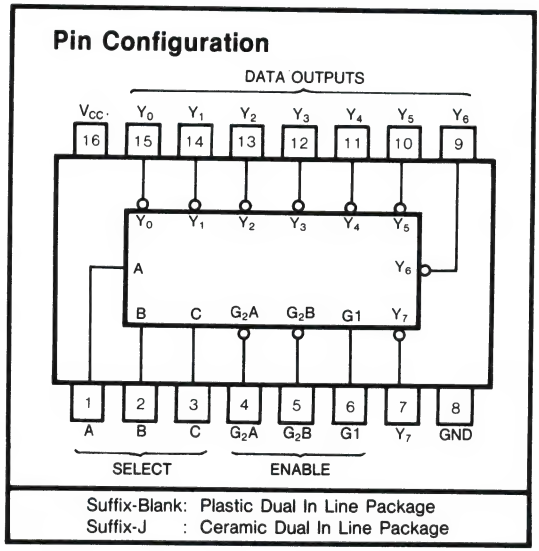
Description

This device is designed to be used in high performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems this decoder can be used to minimize the effects of system decoding. When employd with high-speed memories utilizing a fast enable circuit the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory.

This means that the effect system delay introduced by the schottky-clamped system decoder is negligible.

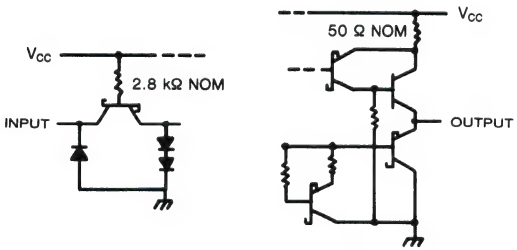
The S138 decodes one of eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverts when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Schematics of Inputs and Outputs



Function Table

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* G2=G2A+G2B

Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min V_{IL}=Max I_{OH}=Max V_{IH}=Min	54	2.5	3.4		V
			74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max I_{OL}=Max V_{IH}=Min				0.5	V
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V, See Note 3			50	90	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	LEVELS of DELAY	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Binary Select	Any	2	C_L=15pF R_L=280Ω		4.5	7	ns
t_{PHL}						7	10.5	
t_{PLH}			3			7.5	12	
t_{PHL}						8	12	
t_{PLH}	Enable	Any	2			5	8	ns
t_{PHL}						7	11	
t_{PLH}			3			7	11	
t_{PHL}						7	11	

* t_{PLH}=propagation delay time, low-to-high-level output* t_{PHL}=propagation delay time, high-to-low-level-output
#For load circuit and voltage waveforms, see page 3-12.

GD54/74S139

DUAL 2-TO-4-LINE DECODERS/DEMULTIPLEXERS

Feature

- Designed Specifically for High Speed:
  - Memory Decoders
  - Data Transmission Systems
- Schottky Clamped for High Performance

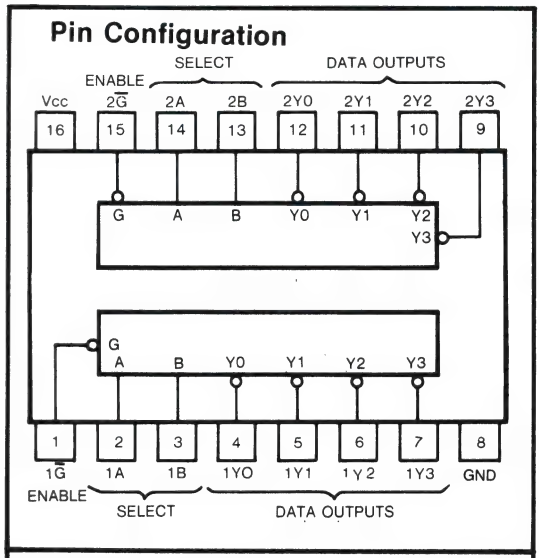
Description

This schottky-clamped TTL MSI circuit is designed to be used in high-performance memory-decoding or data routing applications requiring very short propagation delay times. In high-performance memory systems this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the schottky-clamped system decoder is neglible.

The S139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of the decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Pin Configuration

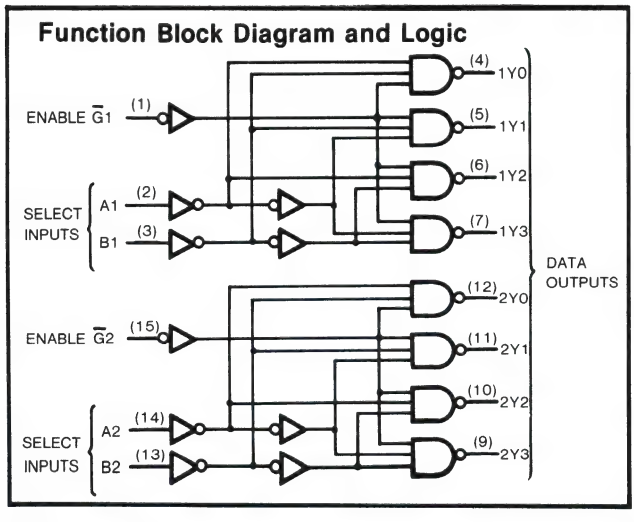


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Function Block Diagram and Logic



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S..... −55°C to 125°C
  74S..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18 mA				−1.2	V
V_{OH}	High level output voltage	V_{CC}=Min V_{IL}=Max	54	2.5	3.4		V
		I_{OH}=Max V_{IH}=Min	74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max I_{OL}=Min V_{IH}=Min				0.5	V
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CC}	Supply current	V_{CC}=Max			60	90	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

PARAMETER*	FROM(INPUT)	TO(OUTPUT)	Levels of Delay	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Binary Select	Any	2	C_L=15pF R_L=280Ω		5	7.5	ns
t_{PHL}			2			6.5	10	
t_{PLH}			3			7	12	
t_{PHL}			3			8	12	
t_{PLH}	Enable	Any	2			5	8	ns
t_{PHL}			2			6.5	10	

#For load circuit and voltage waveforms, see page 3-12.

GD54/74LS153

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

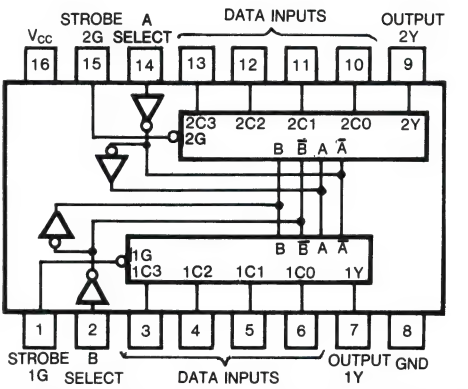
Feature

- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL and DTL Circuits

Description

This monolithic data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip binary decoding data selection to the AND/OR invert gates. Separate strobe inputs are provided for each of the two four line sections.

Pin Configuration

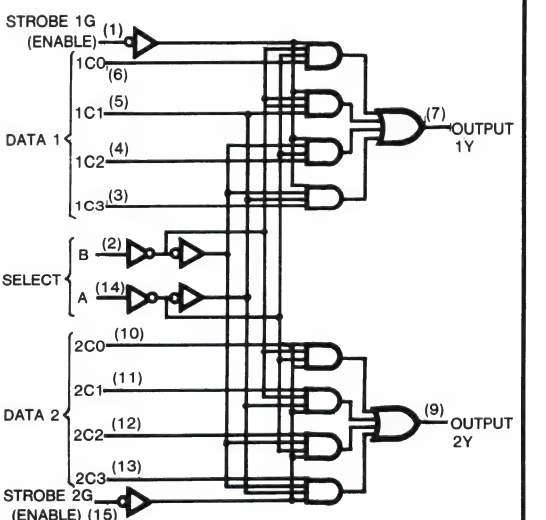


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

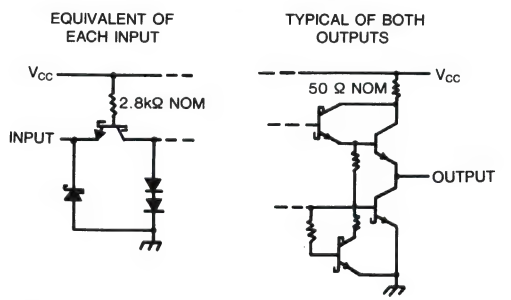
Function Table

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Functional Block Diagram



Schematics of Inputs and Outputs



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min V_{IL}=Max, I_{OH}=Max V_{IH}=Min	54	2.5	3.4		V
			74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max, I_{OL}=Max V_{IH}=Min				0.5	V
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V, (Note 3)			45	70	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with the outputs open, and all inputs ground.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	FROM(INPUT)	TO(OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L=15pF, R_L=280Ω		6	9	ns
t_{PHL}	Data	Y			6	9	ns
t_{PLH}	Select	Y			11.5	18	ns
t_{PHL}	Select	Y			12	18	ns
t_{PLH}	Strobe	Y			10	15	ns
t_{PHL}	Strobe	Y			9	13.5	ns

#For load circuit and voltage waveforms, see page 3-12.

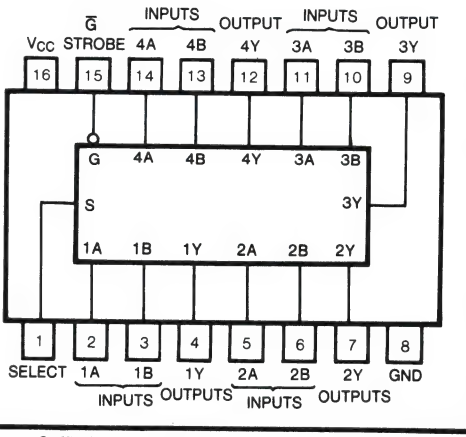
GD54/74S157

QUADRUPLE 2-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

Features

- Buffered Inputs and Outputs
- Schottky clamp provides improved AC performance.
- Selects four of eight data inputs with single select line and over-riding strobe.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Applications

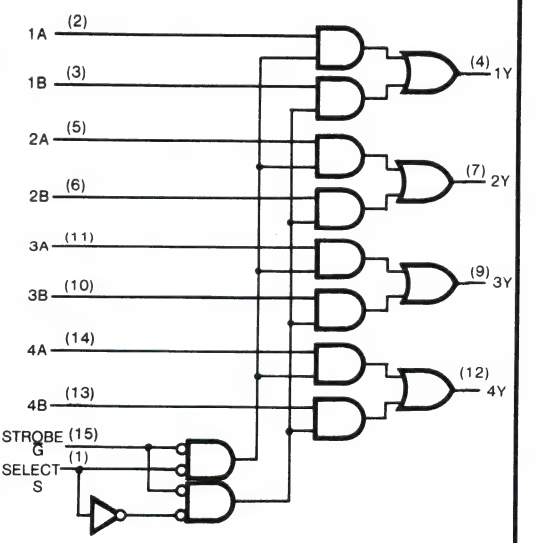
- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables (One Variables is Common)
- Source Programmable Counters

Description

This monolitic data selector/multiplexer contains inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs.

A single select line, S, is used to select one of the two multiplexer input words. When the select is LOW, the A input word is present at the output. When the select is HIGH, the B input word is present at the output.

Function Block Diagram



Function Table

INPUTS				OUTPUT
STROBE	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1	A
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.8	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min, I_{OH}=Max	V_{IL}=Max, V_{IH}=Min	54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, I_{OL}=Max	V_{IL}=Max, V_{IH}=Min				0.5	V
I_I	Input current at maximun input voltage	V_{CC}=Max, V_I=5.5V					1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	S or $\overline{G}$ input				100	μA
			A or B input				50	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V	S or $\overline{G}$ input				−4	mA
			A or B input				−2	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−40		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				50	70	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

PARAMETER*	FROM (INPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Data	C_L=15pF, R_L=280Ω		5	7.5	ns
t_{PHL}				4.5	6.5	
t_{PLH}	Strobe			8.5	12.5	ns
t_{PHL}				7.5	12	
t_{PLH}	Select			9.5	15	ns
t_{PHL}				9.5	15	

* t_{PLH}=propagation delay time, low-to-high-level output.
* t_{PHL}=propagation delay time, high-to-low-level output.
#For load circuit and voltage waveforms, see page 3-12.

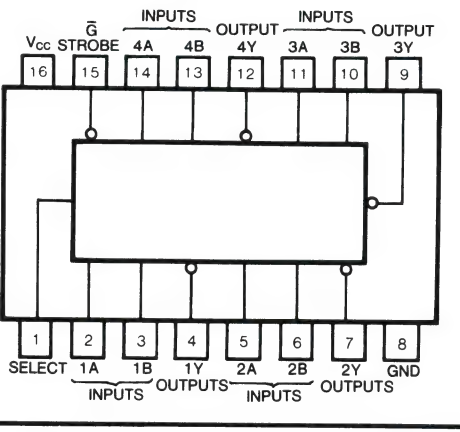
GD54/74S158

QUADRUPLE 2-TO-1-LINE DATA SELECTORS/MULTIPLEXERS (INVERTED DATA OUTPUTS)

Features

- Buffered Inputs and Outputs
- Converted outputs provided.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

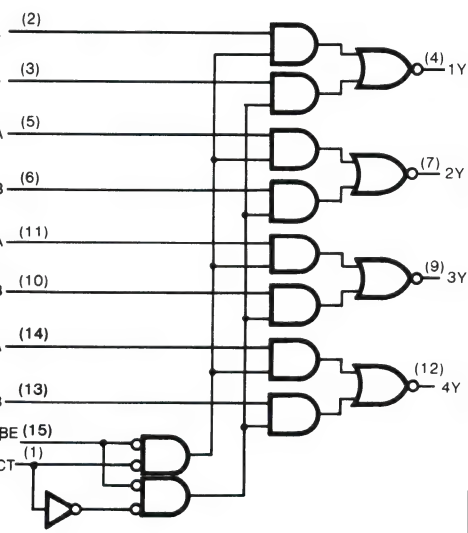
Applications

- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables (One Variables is Common)
- Source Programmable Counters

Description

This monolitic data selector/multiplexer contains inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The S158 presents inverted data to minimize propagation delay time.

Function Block Diagram



Function Table

INPUTS				OUTPUT
STROBE	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.8	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max I_{OL}=Max, V_{IH}=Min					0.5	V
I_I	Input current at maximun input voltage	V_{CC}=Max, V_I=5.5V					1	mA
I_{IH}	High-level input current	V_{CC}=Max	S or $\overline{G}$ input				100	μA
		V_I=2.7V	A or B input				50	
I_{IL}	Low-level input current	V_{CC}=Max	S or $\overline{G}$ input				−4	mA
		V_I=0.5V	A or B input				−2	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−40		−100	mA
I_{CC}	Supply current	V_{CC}=Max	Note 3			39	61	mA
			Note 4				81	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.
Note 4: A inputs at 4.5V, B,G,S, inputs at or, and all outputs open.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

PARAMETER*	FROM (INPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Data	C_L=15pF R_L=280Ω		4	6	ns
t_{PHL}				4	6	
t_{PLH}	Strobe			6.5	11.5	ns
t_{PHL}				7	12	
t_{PLH}	Select			8	12	ns
t_{PHL}				8	12	

* t_{PLH}=propagation delay time, low-to-high-level output.
* t_{PHL}=propagation delay time, high-to-low-level output.
#For load circuit and voltage waveforms, see page 3-12.

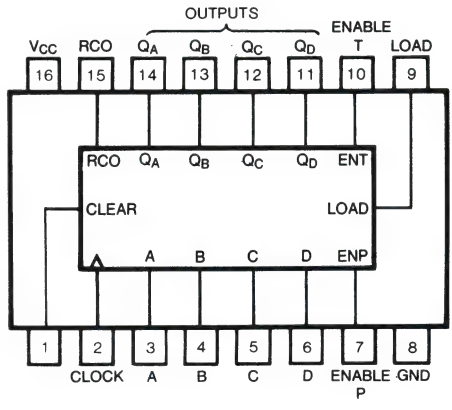
GD54/74S163A

SYNCHRONOUS 4-BIT COUNTER: BINARY, SYNCHRONOUS CLEAR

Feature

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

This synchronous, presettable counter features an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating.
This mode of operation eliminates the outputs counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input with form.

This counter is fully programmable; that is the outputs may be preset to either level. As presetting is synchronous setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.
The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regard less of the levels of the clock, load, or enable inputs

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two counter-enable inputs and a ripple carry output. Both count-enable inputs (ENABLE P and ENABLE T) must be high to count, and ENABLE T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high level portion of the Q_A output. The high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

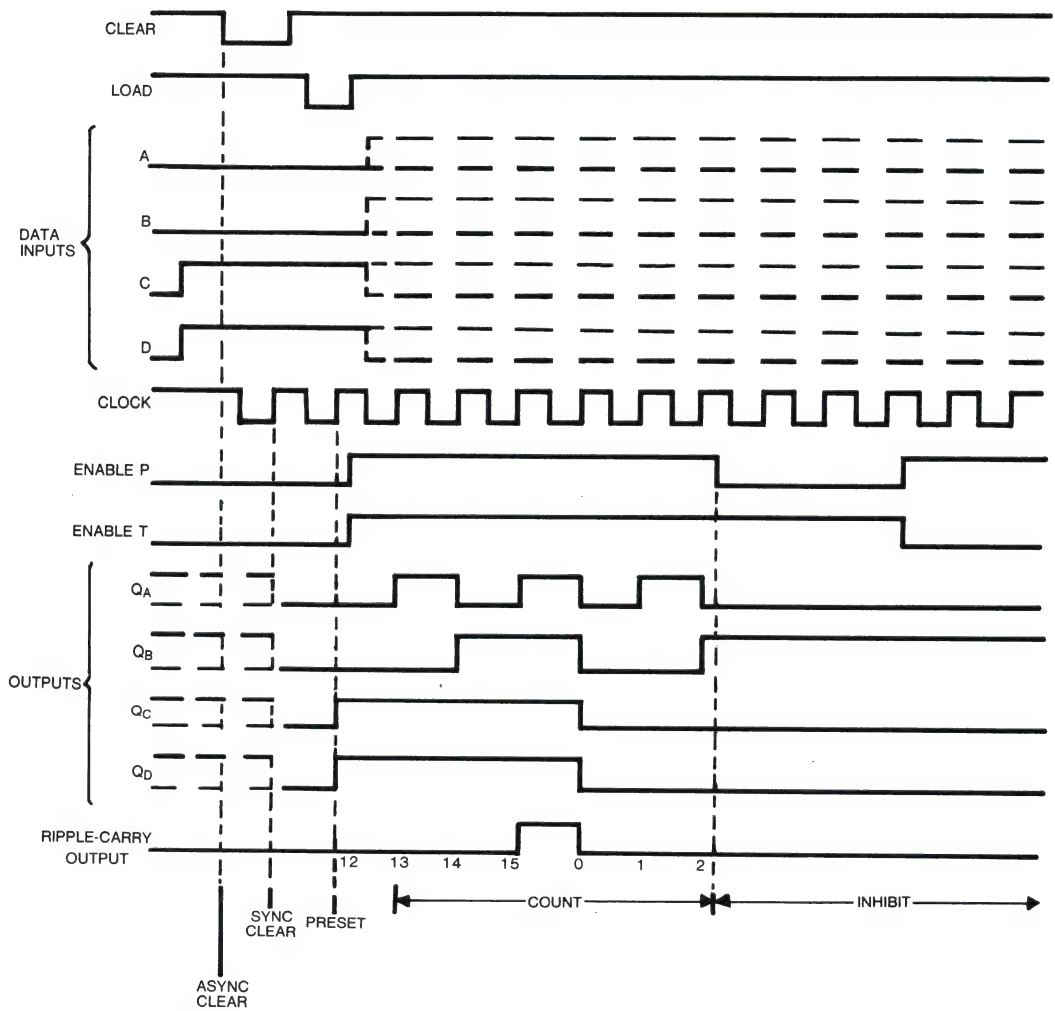
Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Typical, Clear, Preset, Count, and Inhibit Sequences

Illustrated below is the following sequence:

1. Clear outputs to zero (synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit



Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54,74			−1	mA
I_{OL}	Low-level output current		54			20	mA
			74			20	
f_{clock}	Clock frequency			0		40	MHz
t_w	Width of clock or clear pulse			10			ns
$t_{release}$	Width of clear pulse Release time					4	ns
t_{SU}	Setup time	Data inputs A.B.C.D.		4			ns
		Enable P or T		12			
		Load		14			
		Clear		14			
t_h	Hold time	Data		3			ns
		Others		0			
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min	54	2.5	3.4		V
			74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OL}=Max, V_{IH}=Min				0.5	V
I_I	Input current at maximun input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	enable T			100	μA
			other inputs			50	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V	enable T			−4	mA
			other inputs			−2	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CC}	Supply current	V_{CC}=Max			95	160	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

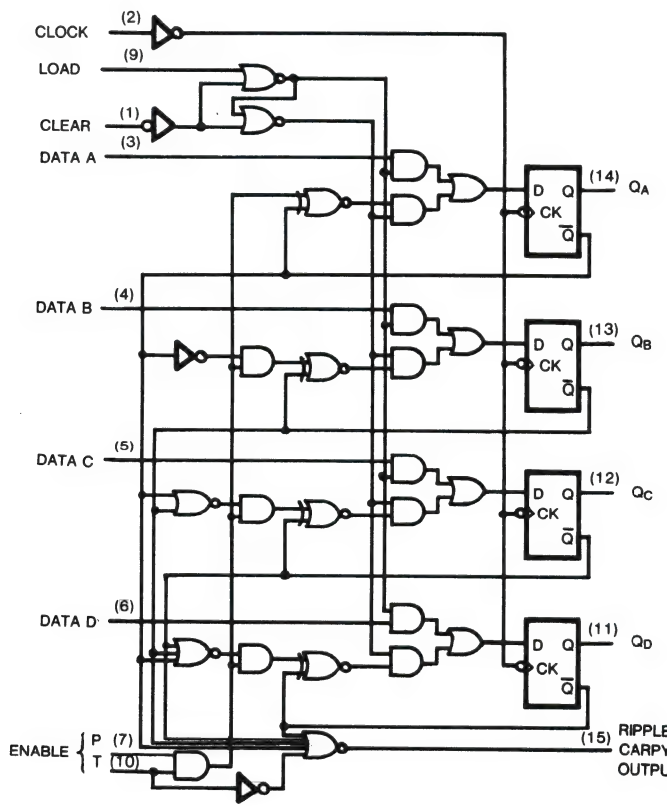
PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}			$C_L=15pF$ $R_L=280\Omega$	40	70		MHz
t_{PLH}	Clock	Ripple carry			14	25	ns
t_{PHL}					17	25	
t_{PLH}	Clock	Any Q			8	15	ns
t_{PHL}					10	15	
t_{PLH}	Enable T	Ripple carry			10	15	ns
t_{PHL}					10	15	

* f_{max}=maximum clock frequency
* t_{PLH}=propagation delay time, low-to-high-level output.
* t_{PHL}=propagation delay time, high-to-low-level output.

Note 1: propagation delay for clearing is measured from the clock transition for the S163A.

#For load circuit and voltage waveforms, see page 3-12.

Function Block Diagram



GD54/74S169A

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

Features

- 'LS169A—binary counter
- Fully synchronous operation for counting and programming.
- Internal look-ahead for fast counting.
- Carry output for n-bit cascading.
- Fully independent clock circuit.

Description

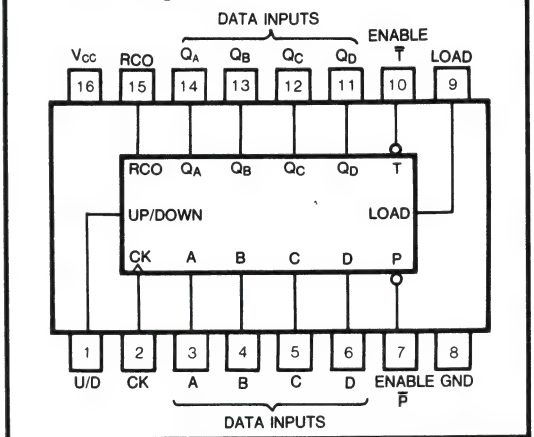
These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all F/Fs-clocked simultaneously, so that the outputs all change at the same time when so instructed by the countenable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load-input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count-enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input 9 When the input is high, the counter counts up; when low, it counts down. Input T is fed forward to enable the carry outputs. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up, and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down), which modify the operating mode, have no effect until clocking occurs. The function of the counter (when enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Mode Select Table

LOAD	$\overline{P}$	$\overline{T}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load ($i \rightarrow Q_i$)
H	L	L	H	Count up
H	L	L	L	Count down
H	H	X	X	No change (Hold)
H	X	H	X	No change (Hold)

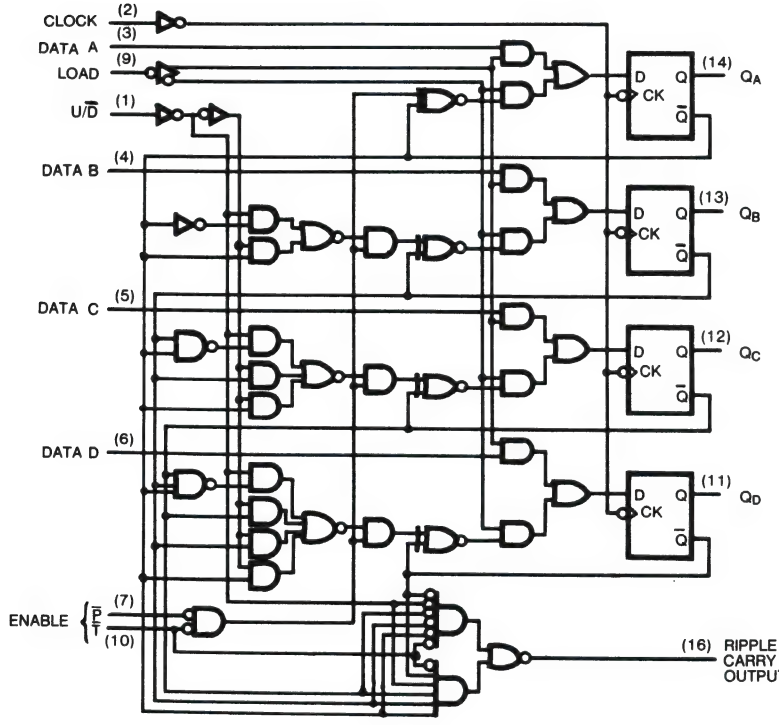
i: Data Inputs
Qi: Outputs

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

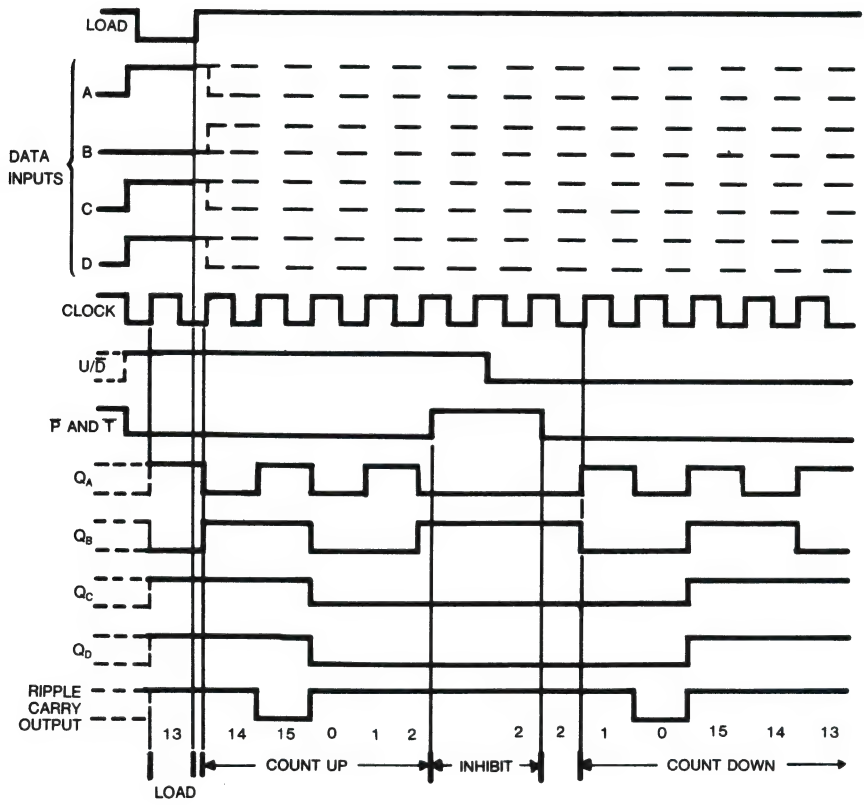
Function Block Diagram

54S169A, 74S169A BINARY COUNTERS



Timing Diagram

S169A Binary Counters
Typical Load, Count, and Inhibit Sequences



Sequence 1: Load (preset) to binary thirteen
Sequence 2: Count up to fourteen, fifteen, zero, one and two
Sequence 3: Inhibit
Sequence 4: Count down to one, zero, fifteen, fourteen and thirteen

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54, 74			−1	mA
I_{OL}	Low-level output current		54			20	mA
			74			20	
f_{clock}	Clock frequecy			0		40	MHz
t_w	Width of clock pulse			10			ns
t_{su}	Set up time	Data inputs A,B,C,D.		4			ns
		Enable $\overline{P}$ or $\overline{T}$		14			
		Load		6			
		Up/Down		20			
t_h	Data hold time			1			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max I_{OL}=Max, V_{IH}=Min					0.5	V
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					1	mA
I_{IH}	High Level Input Current	V_{CC}=Max V_I=2.7V	Load		−10		−200	μA
			Enable $\overline{T}$				100	
			Other inputs				50	
I_{IL}	Low Level Input Current	V_{CC}=Max V_I=0.4V	Enable $\overline{T}$				−4	mA
			Other inputs				−2	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−40		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				100	160	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Note more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured after applying a momentary 4.5V, then ground, is applied to the CLOCK with all other inputs grounded and the outputs open.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}			$C_L=15pF$, $R_L=280\Omega$	40	55		MHZ
t_{PLH}	Clock	Ripple Carry			14	21	ns
t_{PHL}					20	28	ns
t_{PHL}	Clock	Any Q			8	15	ns
t_{PHL}					11	15	
t_{PLH}	Enable $\overline{T}$	Ripple Carry			6	12	ns
t_{PHL}					15	25	
t_{PLH}**	Up/Down	Ripple Carry			8	15	ns
t_{PHL}**					16	22	

* f_{max}=maximum clock frequency.
t_{PLH}=propagation delay time, low-to-high-level output.
t_{PLH}=propagation delay time, high-to-low-level output.
** The propagation delay from UP/DOWN to RIPPLE CARRY must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down Input is changed, the ripple carry output will follow. If the count is minimum, the ripple carry output transition will be in phase. If the count is maximum, the ripple carry output will be out of phase.

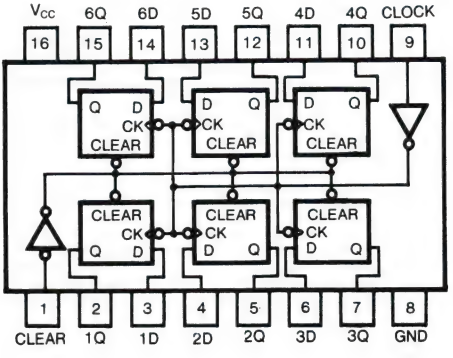
GD54/74S174

HEX D-TYPE FLIP FLOPS SINGLE RAIL OUTPUTS, COMMON DIRECT CLEAR

Feature

- Contains Six Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Application Include: Buffer/Storage Registers
  Shift Registers
  Pattern Generators

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

These monolitic, positive-edge triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positivegoing edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL or DTL circuits.

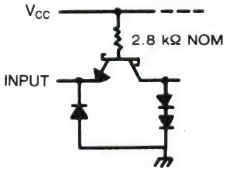
Function Table (each flip-flop)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_O	$\overline{Q}_O$

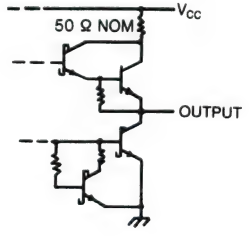
*↑=transition from low to high level.
*Q_O=the level of before the indicated steady state input conditions were established.
X=irrelevant
L=low level (steady state)
H=high level (steady state)

Schematics of Inputs and Outputs

EQUIVALENT OF ALL INPUTS



TYPICAL OF ALL OUTPUTS



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current					−1	mA
I_{OL}	Low-level output current					20	mA
f_{clock}	Clock frequency			0		75	MHz
t_w	Pulse width	Clock		7			ns
		Clear		10			
t_{su}	Set up time	Data input		5			ns
		Clear inactive-state		5			
t_h	Data hold time			3			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min V_{IL}=Max I_{OH}=Max V_{IH}=Min	54	2.5	3.4		V
			74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max I_{OL}=Max V_{IH}=Min				0.5	V
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CC}	Supply	V_{CC}=Max			90	144	mA

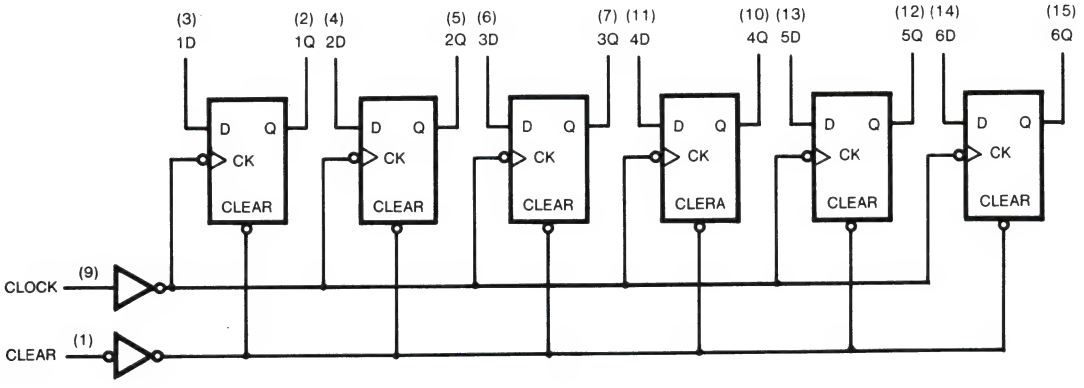
Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L=15pF R_L=2kΩ	75	110		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			13	22	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			11.5	17	ns

#For load circuit and voltage waveforms, see page 3-12.

Function Block Diagram



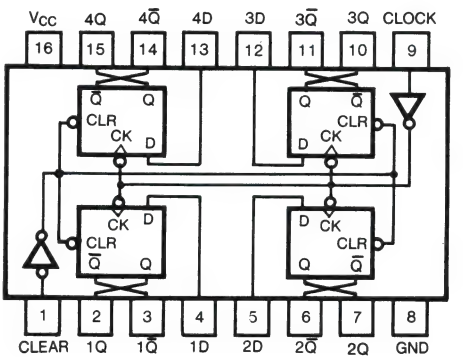
GD54/74S175

QUAD D-TYPE FLIP-FLOPS WITH CLEAR

Features

- Contains Four Flip-Flops with Double-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

This monolithic, positive edge-triggered flip-flops utilize, TTL circuitry to implement D-type flip-flop logic.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

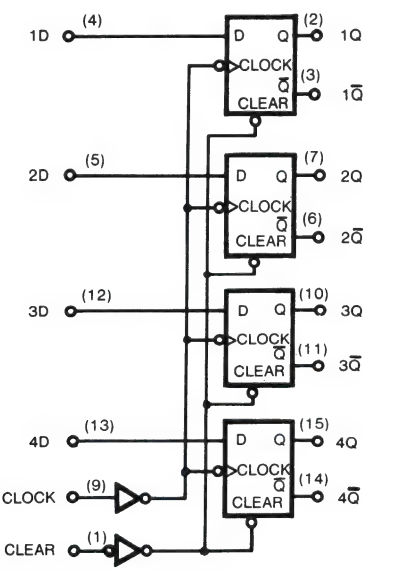
Function Table

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑*	H	H	L
H	↑*	L	L	H
H	L	X	Q_0*	$\bar{Q}_0$

*↑=transition from low to high level

*Q_0=the level of Q before the indicated steady-state input conditions were established.

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}			54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current					−1	mA
I_{OL}	Low-level output current					20	mA
f_{clock}	Clock frequency			0		75	MHz
t_W	Pulse Width	Clock		7			ns
		Clear		10			
t_{SU}	Set up time			5			ns
t_h	Data hold time			3			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High level output voltage	V_{CC}=Min V_{IL}=Max	54	2.5	3.4		V
		I_{OH}=Max V_{IH}=Min	74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max I_{OL}=Max V_{IH}=Min				0.5	V
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)			60	96	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: With all outputs open and 4.5V applied to all DATA and CLEAR inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the CLOCK input.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L=15pF, R_L=2kΩ	75	110		MHz
t_{PLH}	Propagation delay time, low-to-high-level output $\overline{Q}$ from clear			10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output Q from clear			13	22	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			12	17	ns

#For load circuit and voltage waveforms, see page 3-12.

GD54/74S240,S241,S244

OCTAL TRI-STATE BUFFERS/LINE DRIVERS/LINE RECEIVERS

Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins
- Typical I_{OL} (sink current)
  - 54S : 48mA
  - 74S : 64mA
- Typical I_{OH} (Source current)
  - 54S: −12mA
  - 74S: −15mA
- Typical propagation delay times
  - Inverting 4.5 ns
  - Noninverting 6 ns
- Typical enable/disable times 9 ns
- Typical power dissipation (enabled)
  - Inverting 450 mW
  - Noninverting 538 mW

Description

These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanount outputs, and can be used to drive terminated lines down to 133 Ω

Function Tables

54S/74S240

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

54S/74S244

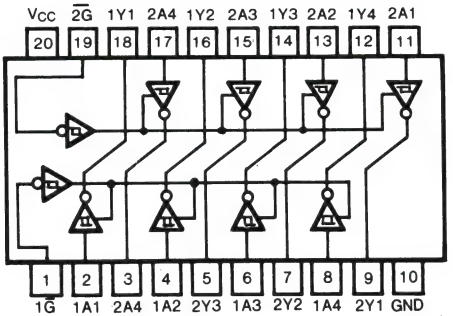
INPUTS		OUTPUT
G	A	Y
H	X	Z
L	H	H
L	L	L

54S/74S241

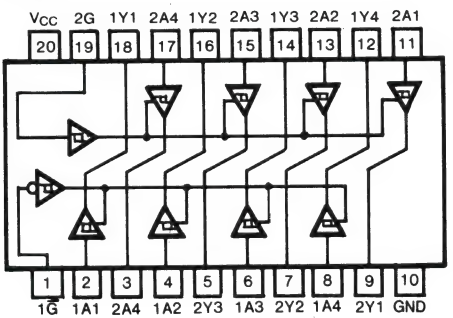
INPUTS			OUTPUTS
$\overline{1G}$	2G	A	Y
H	L	X	Z
L	H	H	H
L	H	L	L

Pin Configuration

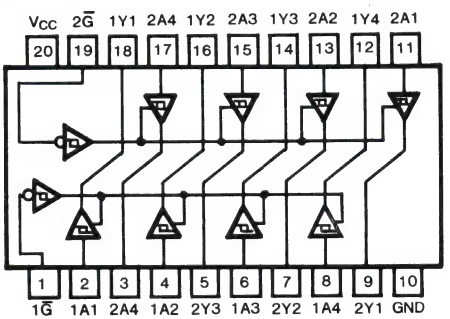
S240



S241

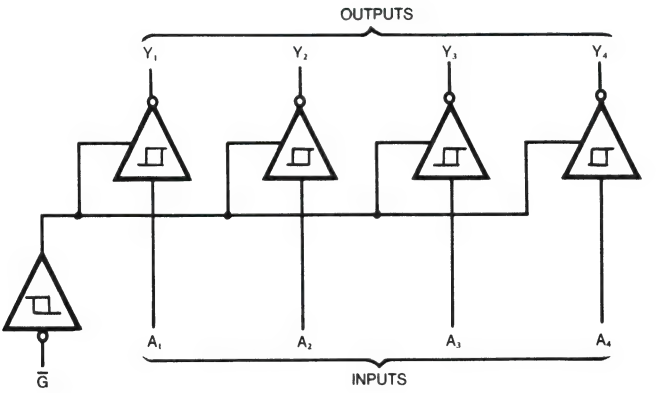


S244

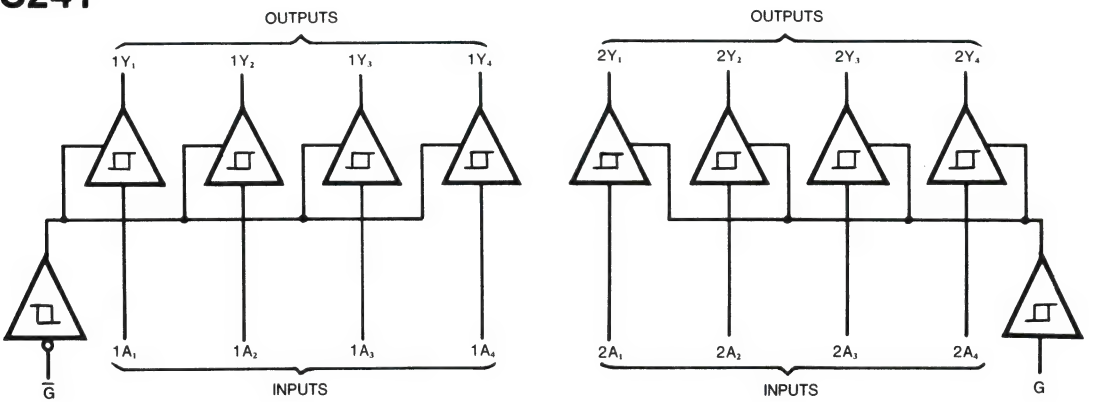


Function Block Diagram

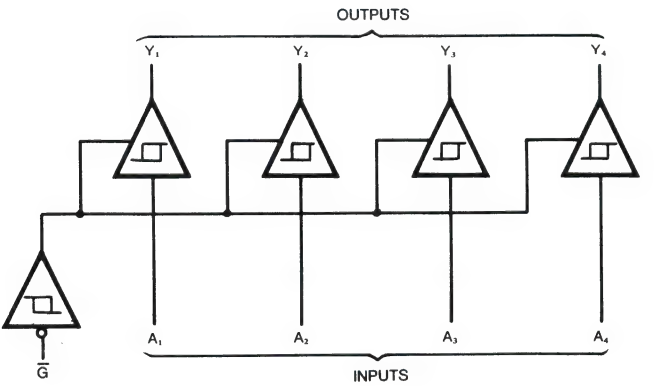
S240



S241



S244



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−12	mA
		74			−15	
I_{OL}	Low-level output current	54			48	mA
		74			64	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High level input voltage			2			V
V_{IL}	Low level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18 mA				−1.2	V
V_{T+}—V_{T-}	Hysteresis	V_{CC}=Min		0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_{IH}=2V V_{IL}=0.8V, I_{OH}=−1 mA		2.7			V
		V_{CC}=Min, V_{IH}=2V V_{IL}=0.8V, I_{OH}=−3 mA		2.4	3.4		
		V_{CC}=Min, V_{IH}=2V V_{IL}=0.5V, I_{OH}=Max		2			
V_{OL}	Low Level Output Voltage	V_{CC}=Min V_{IL}=0.8V, V_{IH}=2V	54			0.55	V
			74			0.55	
I_{OZH}	Off-State Output Current, High-level Voltage Applied	V_{CC}=Max, V_O=2.4V V_{IL}=0.8V V_{IH}=2V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC}=Max, V_O=0.5V V_{IL}=0.8V V_{IH}=2V				−50	μA
I_I	Input Current at Maximum Input Voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High level input current	V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low level input current	V_{CC}=Max, V_I=0.5V	Any A			−400	μA
			Any G			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC}=Max(Note 2)		−50		−225	mA
I_{CC}	Supply Current	Outputs High	54S240		80	123	mA
			74S240		80	135	
			54S241/4		95	147	
			74S241/4		95	160	
		Outputs Low	54S240		100	145	mA
			74S240		100	150	
			54S241/4		120	170	
			74S241/4		120	180	
		Outputs Disabled	54S240		100	145	mA
			74S240		100	150	
			54S241/4		120	170	
			74S241/4		120	180	

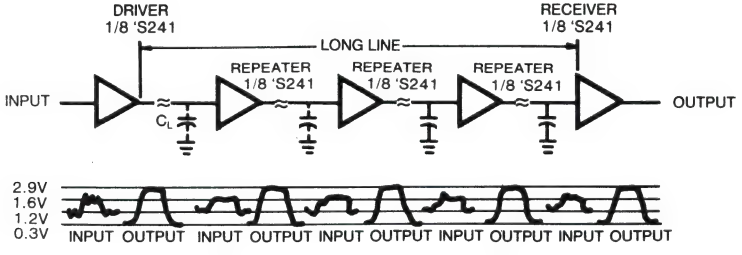
Note 1: All typical values are V_{CC}=5.0V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L=45$ pF $R_L=90\Omega$	54/74S240		4.5	7	ns
			54/74S241,244		6	9	
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L=45$ pF $R_L=90\Omega$	54/74S240		4.5	7	ns
			54/74S241,244		6	9	
t_{PZL}	Output Enable Time to Low Level	$C_L=45$ pF $R_L=90\Omega$	54/74S240		10	15	ns
			54/74S241,244		10	15	
t_{PZH}	Output Enable Time to High Level	$C_L=45$ pF $R_L=90\Omega$	54/74S240		6.5	10	ns
			54/74S241,244		8	12	
t_{PLZ}	Output Disable Time from Low Level	$C_L=5$ pF $R_L=90\Omega$	54/74S240		10	15	ns
			54/74S241,244		10	15	
t_{PHZ}	Output Disable Time from High Level	$C_L=5$ pF $R_L=90\Omega$	54/74S240		6	9	ns
			54/74S241,244		6	9	

APPLICATIONS

54S/74S241'S USED AS REPEATER/LEVEL RESTORER



GD54/74S242, S243

QUADRUPLE BUS TRANSCEIVERS

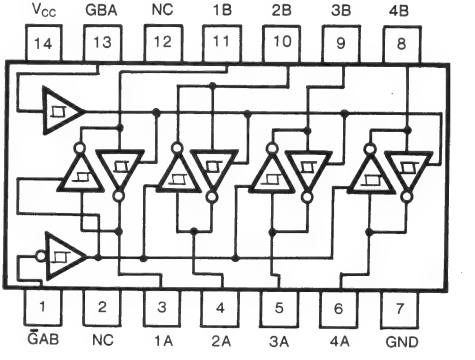
Features

- Two-Way Asynchronous Communication Between Data Buses
- P-N-P Inputs Reduce D-C Loading
- Hysteresis (Typically 400 mV) at Inputs Improves Noise Margin

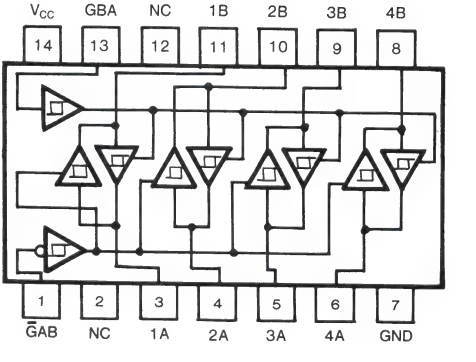
Description

These four data line transceivers are designed for asynchronous two-way communications between data buses. They can be used to drive terminated lines down to 133 ohms.

S242



S243



Function Table

Control Inputs		S242 Data Port Status		S243 Data Port Status	
$\overline{G}$AB	GBA	A	B	A	B
H	H	$\overline{O}$	I	O	I
L	H	*	*	*	*
H	L	ISOLATED		ISOLATED	
L	L	I	$\overline{O}$	I	O

* Possibly destructive oscillation may occur in the transceivers are enabled in both directions at once.
I = Input, O = Output, $\overline{O}$ = Inverting Output

Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−12	mA
		74			−15	
I_{OL}	Low-level output current	54			12	mA
		74			24	
T_A	Operating free-air temperature	54	−55		125	°C
		74	0	70		

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High level input voltage			2			V
V_{IL}	Low level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18 mA				−1.2	V
V_{T+}—V_{T-}	Hysteresis	V_{CC}=Min		0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_{IH}=2V V_{IL}=0.8V, I_{OH}=−1 mA		2.7			V
		V_{CC}=Min, V_{IH}=2V V_{IL}=0.8V, I_{OH}=−3 mA		2.4	3.4		
		V_{CC}=Min, V_{IH}=2V V_{IL}=0.5V, I_{OH}=Max		2			
V_{OL}	Low level output voltage	V_{CC}=Min V_{IH}=2V V_{IL}=0.8V I_{OL}=Max	54		0.25	0.4	V
			74		0.25	0.5	
I_{OZH}	Off-State Output Current, High level Voltage Applied	V_{CC}=Max V_O=2.4V V_{IL}=0.8V V_{IH}=2V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC}=Max V_O=0.5V V_{IL}=0.8V V_{IH}=2V				−50	μA
I_I	Input Current at Maximum Input Voltage	V_{CC}=Max V_I=5.5V				1	mA
I_{IH}	High level input current	V_{CC}=Max V_I=2.7V				50	μA
I_{IL}	Low level input current	V_{CC}=Max V_I=0.5V	Any A			−400	μA
			Any G			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC}=Max(Note 2)		−50		−225	mA
I_{CC}	Supply Current	Outputs High	54S242		80	123	mA
			74S242		80	135	
			54S243		95	147	
			74S243		95	160	
		Outputs Low	54S242		100	145	mA
			74S242		100	150	
			54S243		120	170	
			74S243		120	180	
		Outputs Disabled	54S242		100	145	
			74S242		100	150	
			54S243		120	170	
			74S243		120	180	

Note 1: All typical values are V_{CC}=5.0V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L=45 pF R_L=90Ω	54S242		4.5	7	ns
			74S243		6	9	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L=45 pF R_L=90Ω	54S242		4.5	7	ns
			74S243		6	9	
t_{PZL}	Output Enable Time to Low Level	C_L=45 pF R_L=90Ω	54S242		10	15	ns
			75S243		10	15	
t_{PZH}	Output Enable Time to High Level	C_L=45 pF R_L=90Ω	54S242		6.5	10	ns
			74S243		8	12	
t_{PLZ}	Output Disable Time from Low Level	C_L= 5 pF R_L=90Ω	54S242		10	15	ns
			74s243		10	15	
t_{PHZ}	Output Disable Time from High Level	C_L=5 pF R_L=90Ω	54S242		6	9	ns
			74S243		6	9	

GD54/74S251

DATA SELECTORS/MULTIPLEXEPS WITH 3-STATE OUTPUTS

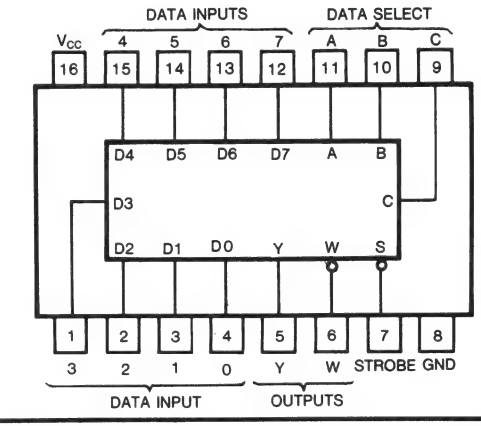
Feature

- Three-State Outputs Interface Directly with System Bus
- Performs Parallel-to-Serial Conversion
- Complementy Outputs Provide True and Inverted Data
- Fully Compatible with Most TTL Circuits

Description

These monorithic data selectors/multiplexers contain full on chip binary decoding to select one-of-eight data sources and feature a strobe controlled three state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit a number of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high impedances state in which both the upper and lower transistors of each totem-pole output are off and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem pole outputs.

Pin Configuration



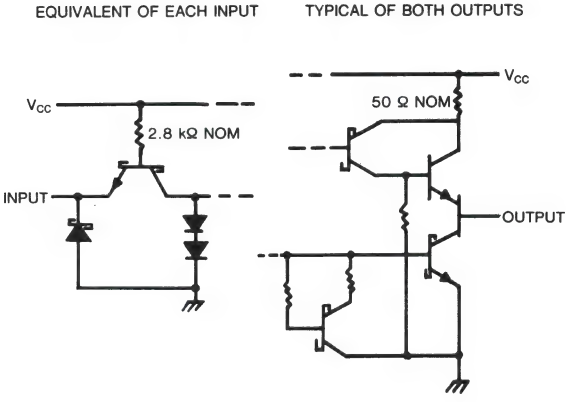
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H=high logic level, L=low logic level
X=irrelevant, Z=high impedance (off)
D0, D1 ...D7=the level of the respective D input

Schematics of Inputs and Outputs



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 5.5V
- Off-state output voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75		5.25	V
I_{OH}	High-level output current			−6.5	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min V_{IL}=Max I_{OH}=Max V_{IH}=Min	54	2.4	3.4		V
			74	2.4	3.1		
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max I_{OL}=Max V_{IH}=Min				0.5	V
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.4V V_{IH}=Min, V_{IL}=Max				50	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.5V V_{IH}=Min, V_{IL}=Max				−50	μA
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V, All inputs at 4.5V All outputs open			55	85	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC}=5V, T_A=25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	A, B or C (4 levels)	Y	C_L=15pF R_L=280Ω		12	18	ns
t_{PHL}					13	19.5	
t_{PLH}	A, B, or C (3 levels)	W			10	15	ns
t_{PHL}					9	13.5	
t_{PLH}	Any D	Y			8	12	ns
t_{PHL}					8	12	
t_{PLH}	Any D	W			4.5	7	ns
t_{PHL}					4.5	7	

#For load circuit and voltage waveforms, see page 3-12.

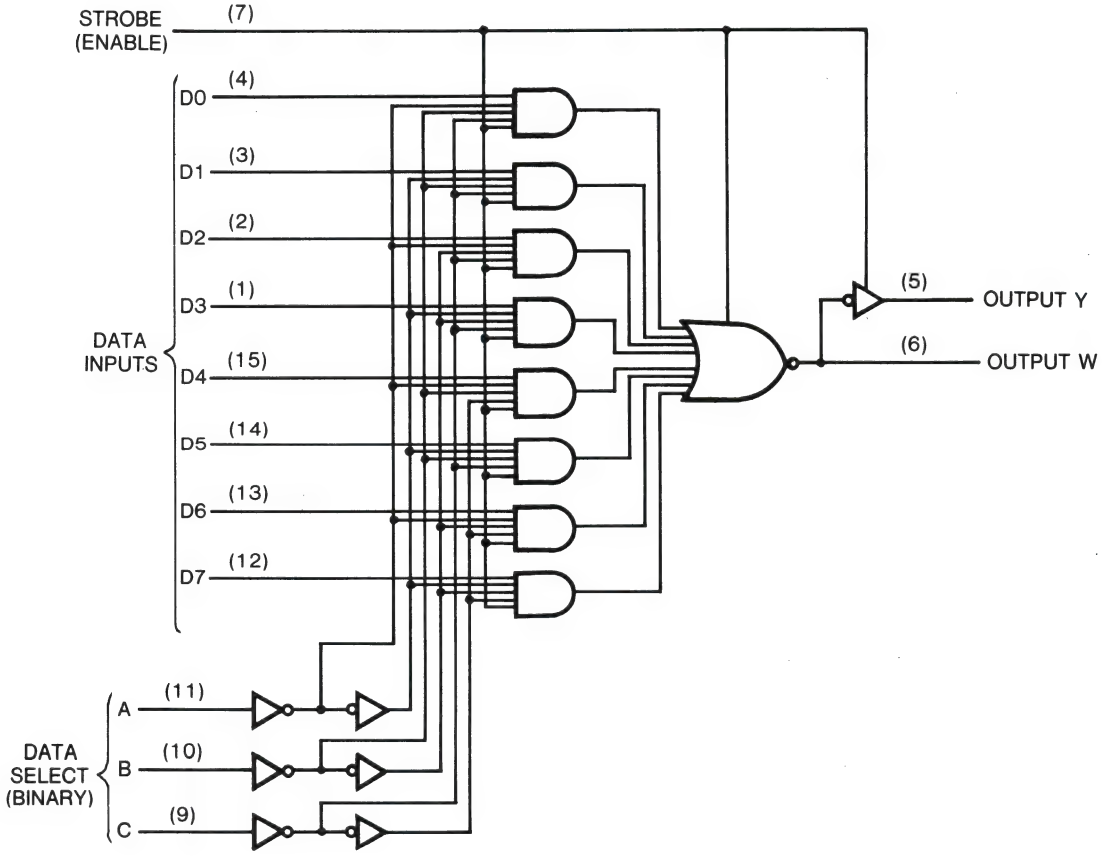
Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PZH}	Storbe	Y	$C_L=50pF$ $R_L=280\Omega$		13	19.5	ns
t_{PZL}					14	21	
t_{PZH}	Strobe	W			13	19.5	ns
t_{PZL}					14	21	
t_{PHZ}	Strobe	Y	$C_L=5pF$ $R_L=280\Omega$		5.5	8.5	ns
t_{PLZ}					9	14	
t_{PHZ}	Strobe	W			5.5	8.5	ns
t_{PLZ}					9	14	

* t_{PLH}=propagation delay time, low-to-high-level output
* t_{PHL}=propagation delay time, high-to-low-leve output
* t_{PZH}=output enable time to high level
* t_{PZL}=output enable time to low level
* t_{PHZ}=output disable time from high level
* t_{PLZ}=output disable time from low level

#For load circuit and voltage waveforms, see page 3-12.

Function Diagram (Positive Logic)



GD54/74S257

QUAD DATA SELECTORS/MULTIPLEXERS: NON-INVERTED 3-STATE OUTPUTS

Features

- TRI-STATE versions S157, S158, with same pin-outs
- Schottky-clamped for significant improvement in A-C performance
- Provides bus interface from multiple sources in high-performance system

Description

These Schottky-clamped high-performance multiplexers feature TRI-STATE outputs that can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common is designed such that the output disable times are shorter than the output enable times.

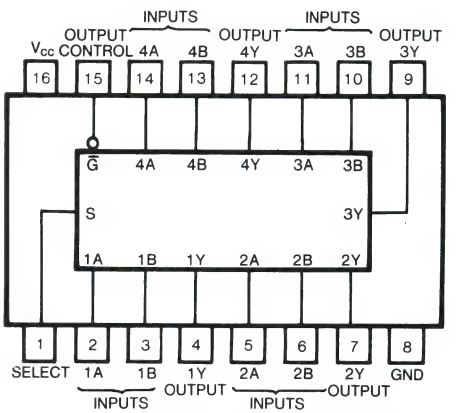
This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

Function Table

INPUTS				OUTPUT
OUTPUT CONTROL	SELECT	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

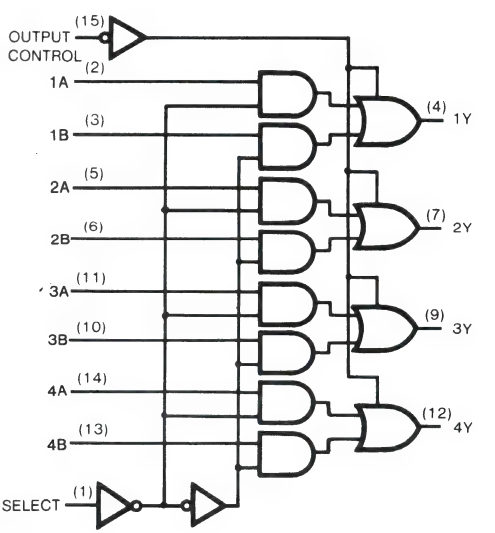
X : Don't care
Z : High Impedance (off)

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54			−2	mA
		74			−6.5	
I_{OL}	Low-level output current	54 74			20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min V_{IL}=Max	54	2.4	3.4		V
		I_{OH}=Max V_{IH}=Min	74	2.4	3.2		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max I_{OL}=Max V_{IH}=Min				0.5	V
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.4V V_{IH}=Min,				50	μA
I_{OZH}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.5V V_{IH}=Min,				−50	μA
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max	S input			100	μA
		V_I=2.7V	Any other			50	
I_{IL}	Low-level input current	V_{CC}=Max	S input			−4	mA
		V_I=0.5V	Any other			−2	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CC}	Supply Current	Outputs high	V_{CC}=5.25V (Note 3)		44	68	mA
		Outputs low			60	93	
		All outputs disabled			64	99	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

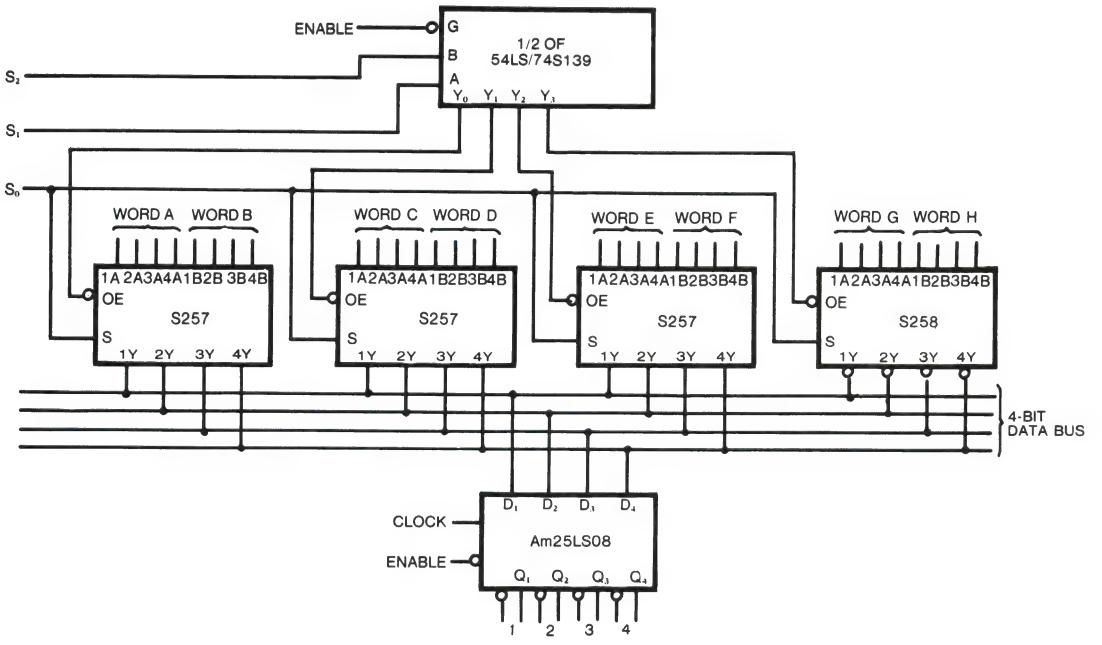
Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Any	$C_L=15$ pF, $R_L=280\Omega$		5	7.5	ns
t_{PHL}					4.5	6.5	
t_{PLH}	Select	Any			8.5	15	ns
t_{PHL}					8.5	15	
t_{PZH}	Output Control	Any			13	19.5	ns
t_{PZL}					14	21	
t_{PHZ}	Output Control	Any	$C_L=5$pF $R_L=280\Omega$		5.5	8.5	ns
t_{PLZ}					9	14	

* t_{PLH} = propagation delay time, low-to-high-level output, t_{PZL} = output enable time to low level
* t_{PHL} = propagation delay time, high-to-low-level output, t_{PHZ} = output disable time from high level.
* t_{PZH} = output enable time to high level, t_{PLZ} = output disable time from low level.
#For load circuit and voltage waveforms, see page 3-12.

Application Example

8-WORD, 4-BIT MULTIPLEXER



GD54/74S280

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

Feature

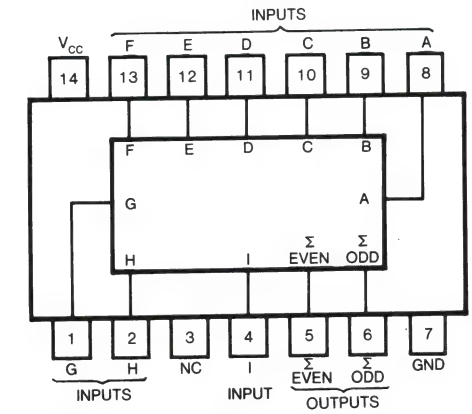
- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits
- Can Be Used to Upgrade Existing Systems Using MSI Parity Circuits

Description

These universal, monolithic, nine-bit parity generators/checkers utilize schottky-clamped TTL high performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity application. The wordlength capability is easily expanded by cascading.

This device can be used to upgrade the performance of most systems utilizing the 180 parity generator/checker. Although the S280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3.

Pin Configuration

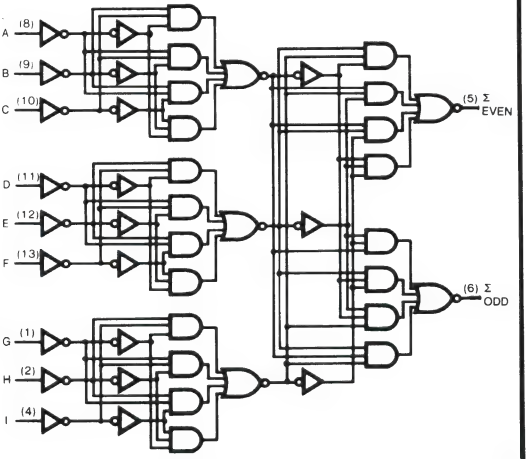


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	ΣODD	ΣEVEN
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

Functional Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S .....−55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current				−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min V_{IL}=Max	54	2.5	3.4		V
		I_{OH}=Max V_{IH}=Min	74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Max, V_{IL}=Max I_{OL}=Max V_{IH}=Min				0.5	V
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)	54		67	99	mA
			74		67	105	

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: I_{CC} is measured with the inputs grounded and outputs open.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Σ Even	$C_L=15pF$, $R_L=280\Omega$		14	21	ns
t_{PHL}					11.5	18	
t_{PLH}	Data	Σ Odd			14	21	ns
t_{PHL}					11.5	18	

* t_{PLH}=Propagation delay time, low-to-high-level output.
t_{PHL}=Propagation delay time, high-to-low-level output.

#For load circuit and voltage waveforms, see page 3-12.

GD54/74S299

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

Features

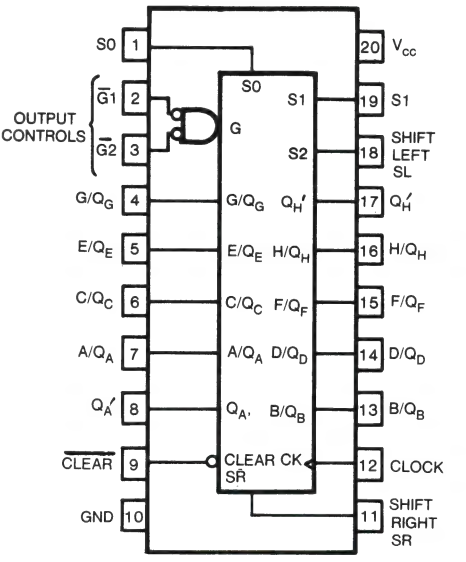
- Synchronous serial/parallel input-serial/parallel input
- Right shift and left shift functions
- Possible expansion of bit number
- 3-state outputs
- Common parallel input and output pins
- Direct reset input

Description

The GD54/74 S299 is a semiconductor integrated circuit containing an 8-bit serial/parallel input-parallel output shift register function equipped with 3-state outputs and direct reset input.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

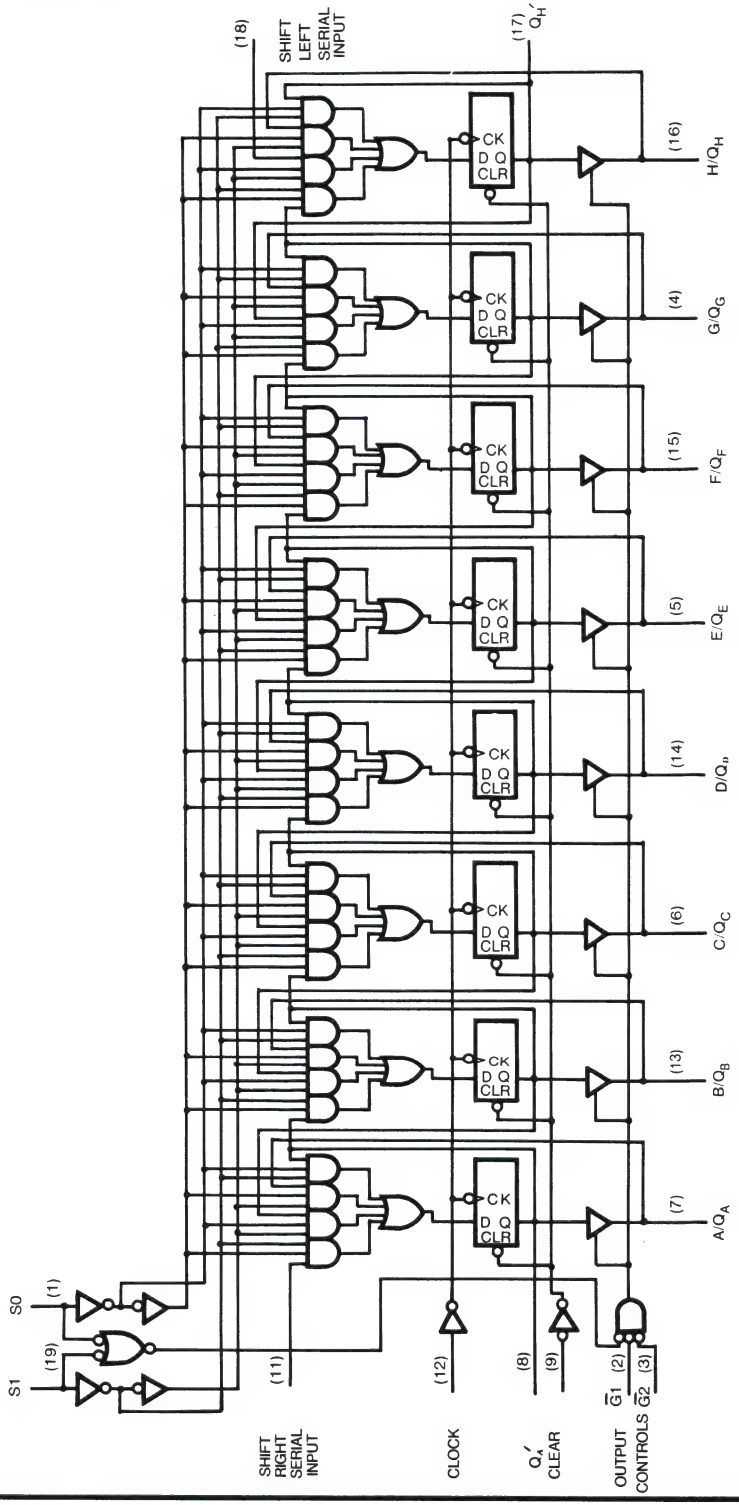
Function Table

MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL*		CLOCK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q'_A	Q'_H
		S1	S0	$\overline{G1}$	$\overline{G2}$	G1	SL	SR										
Clear	L	X	L	L	L	L	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}	Q_{EO}	Q_{FO}	Q_{GO}	Q_{HO}	Q_{AO}	Q_{HO}
	H	X	X	L	L	L	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}	Q_{EO}	Q_{FO}	G_{GO}	Q_{HO}	Q_{AO}	Q_{HO}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

* When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a...h=the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Off-state output voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C t 70°C
- Stoorage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		54S299			74S299			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High Level Output Current (Q_A thru Q_H)				−2			−6.5	mA
	High Level Output Current (Q'_A, Q'_H)				−0.5			−0.5	
I_{OL}	Low Level Output Current (Q_A thru Q_H)				20			20	mA
	High Level Output Current (Q'_A, Q'_H)				6			6	
f_{clock}	Clock Frequency		0		50	0		50	MHz
t_w(clock)	Width of clock pulse	Clock High	10			10			ns
		Clock Low	10			10			
t_w(clear)	Width of clear pulse	Clear Low	10			10			
t_{su}	Setup Time	Select	15↑			15↑			ns
		data High*	7↑			7↑			
		data Low*	5↑			5↑			
		clear inactive state	10↑			10↑			
t_H	Hold Time (Select, Data*)		5↑			5↑			ns
t_{REL}	Clear Release Time		10↑			10↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

* Data includes the two serial inputs and the eight input/output data lines.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I=−18mA			−1.2	V
V_{OH}	High-level output voltage	Q_A thru Q_H	V_{CC}=MIN, V_{IH}=2V, V_{IL}=0.8V, I_{OH}=MAX	2.4	3.2		V
		Q'_A or Q'_H		2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC}=MIN, V_{IH}=2V, V_{IL}=0.8V, I_{OL}=MAX			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	Q_A thru Q_H	V_{CC}=MAX, V_{IH}=2V, V_O=2.4V			100	μA
I_{OZL}	Off-state output current, low-level voltage applied	Q_A thru Q_H	V_{CC}=MAX, V_{IH}=2V, V_O=0.5V			−250	μA
I_I	Input current at maximum input voltage		V_{CC}=MAX, V_I=5.5V			1	mA
I_{IH}	High-level input current	A thru H, S0, S1	V_{CC}=MAX, V_I=2.7V			100	μA
		Any other				50	
I_{IL}	Low-level input current	Clock or $\overline{\text{clear}}$	V_{CC}=MAX, V_I=0.5V			−2	mA
		S0, S1				−400	μA
		Any other				−250	
I_{OS}	Short-circuit output current	Q_A thru Q_H	V_{CC}=MAX (Note 2)	−40		−100	mA
		Q'_A or Q'_H		−20		−100	
I_{CC}	Supply current		V_{CC}=MAX (Note 3)		140	225	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics, V_{CC}=5V, T_A=25°C

PARAMETER	FORM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				50	70		MH_Z
t_{PLH}	Clock	Q'_A or Q'_H	C_L=15pF, R_L=1KΩ,		12	20	ns
t_{PHL}					13	20	
t_{PHL}	$\overline{\text{Clear}}$	Q'_A or Q'_H			14	21	ns
t_{PLH}	Clock	Q_A thru Q_H	C_L=45pF, R_L=280Ω		15	21	ns
t_{PHL}					15	21	
t_{PHL}	$\overline{\text{Clear}}$	Q_A thru Q_H			16	24	ns
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H			10	18	ns
t_{PZL}					12	18	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	C_L=5pF, R_L=280Ω		7	12	ns
t_{PLZ}					7	12	

Note 3: I_{CC} is measured with all outputs open, A, B, and C1 input at 4.5V, and C2, G1, and G2 inputs grounded.

GD54/74S374

OCTAL D-TYPE FLIP-FLOPS; 3-STATE OUTPUTS COMMON OUTPUT CONTROL COMMON CLOCK

Feature

- D-Type-Flops in a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection
- P-N-P Inputs Reduce D-C Loading on Data Lines

Description

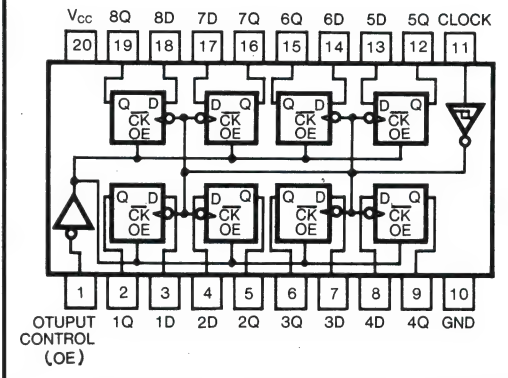
These 8-bit flip-flops feature three-state outputs designed specifically for driving high capacitive or relatively low-impedance loads. This is particulaly suitable for implementing buffer registers, I/O port, bidirectional bus drivers, and working registers.

The eight flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs will be set to the logic levels that were set up at the D inputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull up components.

The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Pin Configuration

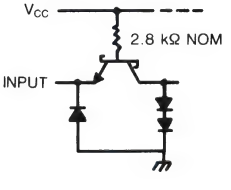


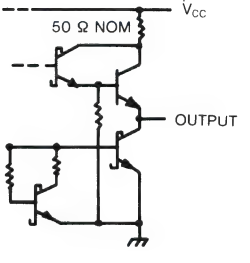
Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_O
H	X	X	Z

Schematics of Inputs and Outputs





Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C
- Off-state output voltage 5.5V

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	V
V_{OH}	High-level output voltage				5.5	V
I_{OH}	High-level output current	54			−2	mA
		74			−6.5	
I_{OL}	Low-level output current				20	mA
t_W	Width of clock or enable pulse	High	6			ns
		Low	7.3			
t_{SU}	Data setup time		5†			ns
t_h	Data hold time		2†			ns
t_A	operating free-air temperature	54	−55		125	°C
		74	0		75	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min V_{IL}=Max I_{OH}=Max V_{IH}=Min	54	2.4	3.4		V
			74	2.4	3.1		
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max I_{OL}=Max V_{IH}=Min				0.5	V
I_{OZH}	Off-state output current high-level voltage applied	V_{CC}=Max, V_O=2.4V V_{IH}=Min, V_{IL}=Max				50	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC}=Max, V_O=0.5V V_{IH}=Min, V_{IL}=Max				−50	μA
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V				−250	μA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V			90	140	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

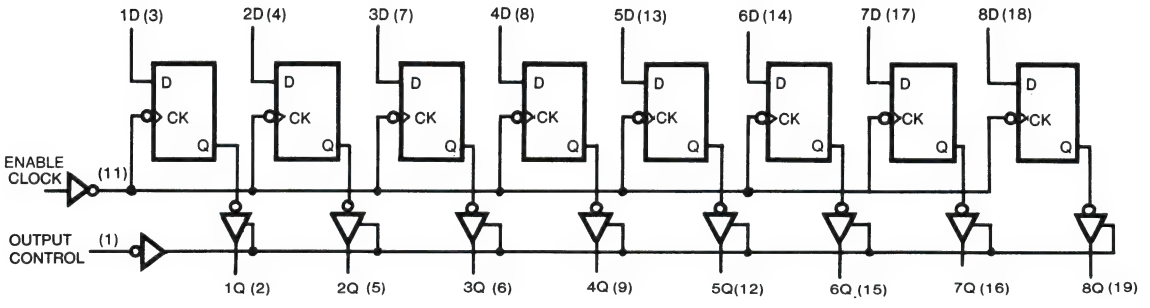
PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}			$C_L=15pF$, $R_L=280\Omega$	75	100		MHz
t_{PLH}	Clock or enable	Any Q			8	15	ns
t_{PHL}					11	17	
t_{PZH}	Output control	Any Q	$C_L=15pF$, $R_L=280\Omega$,		8	15	ns
t_{PZL}					11	18	
t_{PHZ}	Output control	Any Q	$C_L=5pF$, $R_L=280\Omega$ (Note 1)		5	9	ns
t_{PLZ}					7	12	

* f_{max}=maximum clock frequcncy
t_{PLH}=propagation delay time, low-to-high-level output
t_{PHL}=propagation delay time, high-to-low-level output
t_{PZH}=output enable time to high level
t_{PZL}=output enable time to low level
t_{PHZ}=output disable time from high level
t_{PLZ}=output disable time from low level

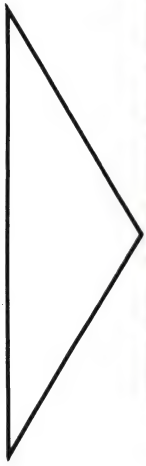
Note 1: maximum clock frequency is tested with all outputs loaded

#For load circuit and voltage waveforms, see page 3-12.

Function Block Diagram



NUMERICAL/FUNCTIONAL INDEX 1
FUNCTIONAL INDEX/SELECTION GUIDE 2
TTL CHARACTERISTICS 3
GD74LS FAMILY CIRCUITS 4
GD74S FAMILY CIRCUITS 5
QUALITY ASSURANCE MANUAL 6
ORDERING INFORMATION & PACKAGE DIMENSION 7
GOLDSTAR SEMICONDUCTOR SALES NETWORK 8



QUALITY ASSURANCE MANUAL

1. INTRODUCTION
2. QUALITY ASSURANCE SYSTEM
   - 2.1 Quality Assurance at the Development State
   - 2.2 Quality Assurance at the Mass Production State
     - — 2.2.1 Control of Material Purchasing
     - — 2.2.2 Control of The Manufacturing Process
     - — 2.2.3 Environment Control
     - — 2.2.4 Control of Production and Instrument
3. RELIABILITY TEST
   - 3.1 Principle of Reliability
   - 3.2 Reliability Test Items and Conditions
4. SUMMARY
5. HANDLING AND STORAGE INSTRUCTION

1. INTRODUCTION

In recent years, advances in intergrated circuit have been rapid with increasing density and speed accompanied by decreasing cost. To meet these advances, there are three basic ingredients in the manufacture of reliable integrated circuits.

First, The device must be designed with the user's applications and reliability reguirements in mind.
Secondly, The device must be manufactured with the optimum technology for the application.
Thirdly, Controls must be established to assure maintenance of the quality/reliability levels.
Goldstar Semiconductor has a Quality Assurance System and conducts extensive reliability testing to supply it's customer's needs.
This report presents Quality Assurance System and Reliability test results of Goldstar Semiconductor Company Products.

2. QUALITY ASSURANCE SYSTEM

To ensure that customers are satisfied with the products that are supplied, quality assurance programs are used at both the design and manufacturing phases, focusing on the following points:

(1) In the development stase, reliability is designed into products. A through evaluation of reliability is performed to ascertain whether the design will lead to the desired quality and reliability.
(2) Efforts are made at the manufacturing stage of quality control to assure that quality and reliability are built into products. Intermediate, final, and quality assurance inspection are used to verify that the desired quality and reliability have been achieved.
(3) Information with regard to quality is fed back in a timely manner so that the required corrective action can be taken by quality assurance personal.

2.1 Quality Assurance at the Development Stage

It is not an exaggeration to say that the fundermental quality and reliability of a discrete semiconductor device or an intergrated circuit is determined at the design stage. Thus, to eliminate design problems and provide design improvements while attaining the desired quality and reliability, design reviews are performed on prototypes assure product quality. Particularly in the case of intergrated circuits, breadboard models of the circuit using standard components can be an effective means of evaluating the required characteristic and quality. In addition CAD technology may be used to aid in the design of circuits and devices based on design standards.

Between the development stage, and mass production, there are two steps of prototype and preproduction (trial mass production).

At the prototype development stage, new theories, technologies and concepts are used by the development department to design and produce a new product. To determine whether the desired goals for characterstics, ratings, and reliability have been met, primary type test is performed at this stage. Based on these results, thorough investigations are made by both the engineering and quality assurance departmanents. Should product deficiencies arise, inspections and failure analysis are performed to enable improvements of the development prototype.

At the pre-production stage, the production department produces sufficient products having quality equal to or superior to the prototype. At this stage, secondary type test is used to verify quality. The required product specifications, operation instructions, drawings, etc., are produce at this stage in addition to the required manufacturing facilities.

2.2 Quality Assurance at the Mass Production Stage

At the mass production stage, the production department takes over production of product based on production planning. To maintain equal or better quality than that obtained in previous stages, carefull control of materials purchasing, production processing, environment and facilities is performed. In addition, in process inspections and final inspections provide the required information with regard to partiality completed and completed devices to assure overall quality.

2.2.1 Control of Materials Purchasing

While the responsibility for quality of individual materials purchased from vendors based on drawings and purchase specifications is the responsibility of the vendor, the corporation provides data from incoming inspection of sampled products as a means of monitoring quality and assuring materials quality.

Selection of vendors is made adopter an investigation of quality control, management, facilities and production capacity of the vendor, placing heavy emphasis on quality. Next, a meeting is held with the vendor concerning the purchase specifications, and prototypes or sample evaluations are used to verify quality at the beginning or a purchase cycle or after a change in manufacturing method or specifications.

2.2.2 Control of the Manufacturing Process

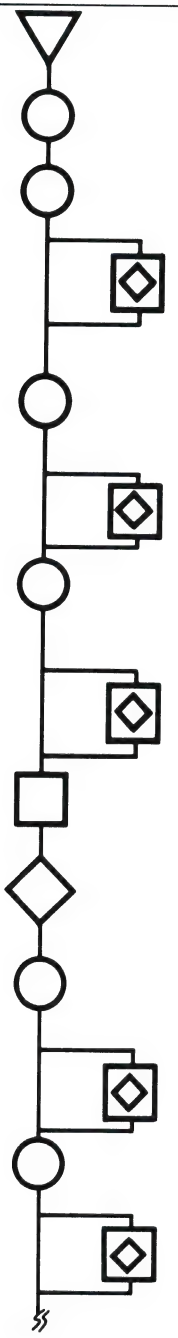
To prototype products of high quality in an economic manner, quality must be built-in at the manufacturing stage. To do this, work is carried out in accordance with operation instructions and check sheets are used to control those aspects of manufacturing that could affect quality. For example, such information as the purity of water, atmosrhere, furnace temperature and gas flow are recorded. In addition, because of their great influence on diffusion, diffusion depth and surface density are recorded and used as control data for process conditions. Also, operations such as wire bonding which are affected by differences of individuals have been fully automated to contribute to product uniformity.

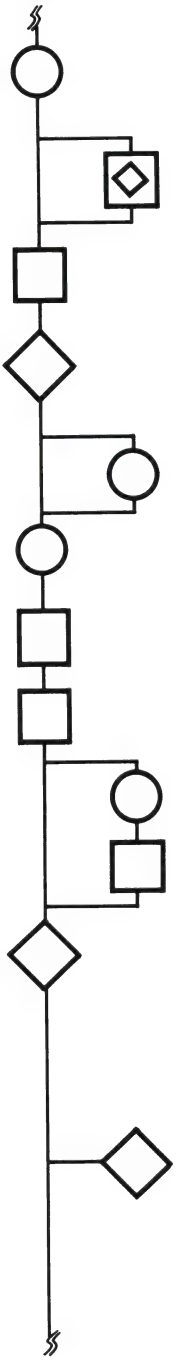
In-process inspections and final inspections are performed to evaluate product quality including outward appearance, dimensions, structure, as well as mechanical and electrical characteristics. The data obtained by such inspections is fed back to earlier processes to maintain and improve product quality as well as reduce variations in these areas.

Wafer processing and assembly inspections are part of the in-process inspection program, each contributing to the concept of building in quality at the manufacturing stage by providing self checks and the inspections performed by the quality control dopartment. A final inspection of all products is performed to verify electrical characteristics as well as outward appearance of products. In addition, to improve product quality uniformity, debugging is used as a means of eliminating products which do not meet quality specifications. Again, data from these inspections are useful in quality control.

Products which have passed final inspection are then subjected to quality assurance inspections. This is a form of overall inspection from the standpoint of the end user and is used to accept or reject products on a lot basis, including tests of outward appearance, electrical characteristics, thermal and mechanical environment, and endurance. As an additional control test, samples are made periodically for evaluation of reliability. These tests include those of electrical characterics, thermal and mechanical environment, and endurance for long periods of operation. The information on quality obtained by such quality assurance inspections is fed back in a timely fashion to the related departments, enabiling the maintenance and improvement of quality as well as providing a means of predicting product quality in the market palce.

STANDARD ASS'Y FLOW CHART OF GSS

FLOW CHART	PROCESS TITLE	QC POINT
	Wafer	
	Foil Mount	
	Wafer Sawing	
	Q.C Monitor * DI Water * Visual	RESISTIVITY VISIUAL
	Die Bond	
	Q.C Monitor * Visual * Die Shear	APPEARANCE STRENGTH
	Wire Bond	
	Q.C Monitor * Visual * Bond pull * Crater	APPEARANCE APPEARANCE, STRENGTH CRATER
	3rd Optical Insp.	
	Q.C 3/0 gate * Visual	APPEARANCE
	Molding	SPRIAL FLOW
	Q.C Monitor * Visual * X-Ray Monitor	APPEARANCE X-RAY INSP.
	Deflash/Trim/Form	
	Q.C Monitor * Visual/Dimension	APPEARANCE/DIMENSION

FLOW CHART	PROCESS TITLE	QC POINT
	Solder-Dipping	
	Q.C Monitor * Temp of S/Bath * Sn in Solder * Solderability	TEMPERATURE. % OF Sn APPEARANCE
	4th Optical Insp	
	4th O/Gate * Visual	APPEARANCE
	Temp. cycle (Option)	
	Mark & Cure	
	Final Visual/Mech.	
	Initial Class	
	Burn-In (Option)	
	Final Test	
	Q.C Final Gate * Visual	APPEARANCE
	* Electrical	ELECTRICAL PARAMETERS * D.C & SPEED * FUNCTION
	RELIABILITY TEST * LIFE TEST LTPD: 5% * 85/85 TEST LTPD: 10% * PRESSURE POT LTPD: 10% * THERMAL SERIES LTPD: 10% * LEAD INTEGRITY LTPD: 20% * PHYSICAL DIMENSION LTPD: 15%	ENVIRONMENTAL TEST MECHANICAL TEST AND ENDURANCE TEST

FLOW CHART	PROCESS TITLE	QC POINT
	* RESISTANCE TO SOLVENTS LTPD: 15% * SOLDERABILITY LTPD: 10% Packing Q.C Pack Gate Ship * ESD MONITOR (ALL PROCESS)	

2.2.3 Environmental Control

In the semiconductor industry, the environment plays a large role in influencing product quality and reliability. Control levels for dust, humidity, and temperature are set and rigidly maintained. The gases or water used in the production plant are carefully controlled to ensure high level of purity.

The control of dust is particularly important in reducing manufacturing defects and improving quality and reliability. For this reason the Corporation places heavy emphasis in this area, providing strict controls of working conditions and periodic checks to varify that these are being maintained.

2.2.4 Control of Production Equipment and Instrumentation.

The semiconductor industry is an equipment intensive industry having adopted a large variety of automatic equipment and high performance facilities to provide uniform high quality. The control of such equipment and instrumentation is extremely important in the manufacture of devices. For this reason, to eliminate loss of accuracy and equipment failures, periodic preventive maintenance and inspections are performed.

3. RELIABILITY TEST

3.1 Principle of Reliability

The fundermental principles of reliability engineering predict that the failure rate of any group of devices as a function of time will follow a curve similar to Figure 1. The curve is divided into three regions: Infant Mortality, Random Failures and Wearout Failures. These regions describe the principal classes of failure mechanisms encountered in that portion of the life of a device.

Infant Mortality represents the early life failures of a device. Failures in this region are usually associated with one or more manufacturing defects. After some period of time the failure rate reaches a low value or the Random failure portion of the curve that represents the useful portion of device life. Infant Mortal

failures are eliminated prior to customer shipment by high voltage cell stress, HTRB and reliability screen testing. (Baking, Temp Cycle, Burn-IN)

Wearout failures occur at the end of the device's useful life and are characterized by rapidly rising failure rate with time. This does not occur before hundreds of years for integrated circuits.

Associated with each portion of the curve are specific failure mechanisms. These failure mechanisms have been extensively discussed in the literature.

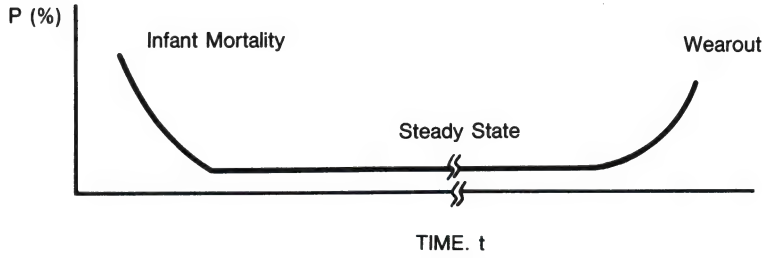


Figure 1. Reliability Life (Bath-tub) Curve

3.2 Reliability Test Items and Conditions

I. Group A: ELECTRICAL TEST

TEST ITEMS.	METHOD.	MIL-STD-883C	GOLDSTAR SEMI.
1. STATIC TEST (AT 25°C)		LTPD 2 : S/S = 266 C = 26	
2. STATIC TEST (AT MAX. OP. TEMP.)		LTPD 3 : S/S = 176 C = 2	AQL = 0.04% S/S = 315 C = 0
3. STATIC TEST (AT MIN. OP. TEMP.)		LTPD 5 : S/S = 105 C = 2	
4. DYNAMIC TEST (AT 25°C)		LTPD 2 : S/S = 266 C = 2	
5. DYNAMIC TEST (AT MAX. OP. TEMP.)		LTPD 3 : S/S = 176 C = 2	
6. DYNAMIC TEST (AT MIN. OP. TEMP.)		LTPD 5 : S/S = 105 C = 2	
7. FUNC. TEST (AT 25°C)		LTPD 2 : S/S = 266 C =2	
8. FUNC. TEST (AT MAX. MIN OP. TEMP.)		LTPD 5 : S/S = 105 C = 2	
9. SWITCHING (AT 25°C)		LTPD 2 : S/S = 266 C = 2	
10. SWITCHING (AT MAX. OP. TEMP.)		LTPD 3 : S/S = 176 C = 2	
11. SWITCHING (AT MIN. OP. TEMP.)		LTPD 5 : S/S = 105 C = 2	

II. Group B : Per Lot

TEST ITEMS.	METHOD.	MIL-STD-883C	GOLDSTAR SEMI.
Sub 1			
PHYSICAL DIMENSION	2016	n = 2 : c = 0	n = 2 : c = 0
Sub 2			
RESISTANCE TO SOLVENTS	2015	n = 4 : c = 0	LTPD 15% S/S = 15 C = 0
Sub 3			
SOLDERABILITY TEST	2022 2003	LTPD 15% S/S = 15 C = 0	LTPD 10% S/S = 22 C = 0
Sub 4			
INTERNAL VISUAL & MECHANICAL	2014	n = 1 : c = 0	n = 1 : c = 0
Sub 5			
BOND STRENGTH	2011	LTPD 15% S/S = 15 C = 0	LTPD 15% S/S = 15 C = 0
Sub 6			
INTERNAL WATER VAPOR CONTENT	1018	n = 3 : c = 0 or n = 5 : c = 1	NOT BEING
Sub 7			
SEAL			
FINE LEAK GROSS LEAK	1014	LTPD 5% S/S = 45 C = 0	LTPD 5% S/S = 45 C = 0
Sub 8			
A) ELECTRICAL PARAMETERS	Gr A	n = 15 : c = 0	LTPD 10% S/S = 22
B) E. S. D CLASSIFICATION	3015		C = 0
C) ELECTRICAL PARAMETERS	Gr A		

III. Group C : PERIODIC : DIE-RELATED TESTS

TEST ITEMS.	METHOD.	MIL-STD-883C	GOLDSTAR SEMI.
Sub 1			
A) STEADY STATE LIFE TEST	1005	AT 125°C : 1000 HRS	AT 125°C : 1000 HRS
B) END POINT ELECTRICAL.		LTPD 5% S/S = 77 C = 1	LTPD 5% S/S = 77 C = 1
Sub 2			
A) TEMPERATURE CYCLE	1010	TEST COND. C LTPD 15% S/S = 25, C = 1	TEST COND. C : 100 CYCLE LTPD 15% S/S = 25, C = 1
B) CONSTANT ACCELERATION	2001	TEST COND. E Y1 ORIENTATION ONLY	TEST COND. E Y1 ORIENTATION ONLY
C) SEAL	1014		
FINE LEAK		TEST COND. B	TEST COND. B
GROSS LEAK		TEST COND. C	TEST COND. C
D) VISUAL EXAMINATION	1010 1011		
E) END POINT ELECTRICAL.			

IV. Group D : PACKAGE RELATED TESTS

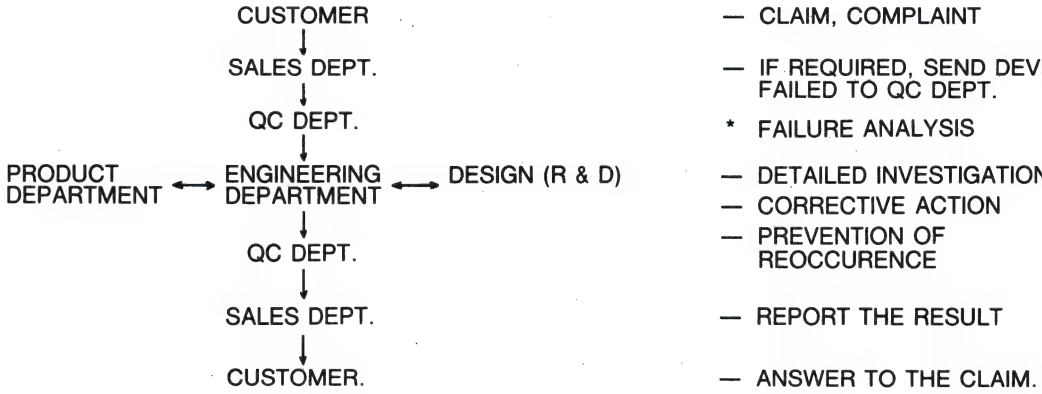
TEST ITEMS.	METHOD.	MIL-STD-883C	GOLDSTAR SEMI.
Sub 1 PHYSICAL DIMENSION	2016	LTPD 15% S/S = 15 C = 0	LTPD 15% S/S = 15 C = 0
Sub 2 A) LEAD INTERGRITY	2004	LTPD 15% S/S = 15 C = 0	LTPD 15% S/S = 15 C = 0
B) SEAL	1014		
FINE LEAK		TEST COND. B	TEST COND. B
GROSS LEAK		TEST COND. C	TEST COND. C
Sub 3 A) THERMAL SHOCK	1011	COND. B : 15 CYCLES LTPD 15% S/S = 15 C = 0	NOT BEING
B) TEMPERATURE CYCLE	1010	TEST COND. C : 100 CYCLE	TEST COND. C : 100 CYCLE
C) MOISTURE RESISTANCE	1004		
D) SEAL	1004		
FINE LEAK		TEST COND. B	TEST COND. B
GROSS LEAK		TEST COND. C	TEST COND. C
E) VISUAL EXAMINATION	1010 & 1004		
F) END POINT ELECTRICAL.			
Sub 4 A) MECHANICAL SHOCK	2002	LTPD 15% S/S = 15 COND.B C = 0	LTPD 15% S/S = 15 COND B C = 0
B) VIBRATION, VARIABLE FREQUENCY	2007	TEST COND. A	TEST COND. A
C) CONSTANT ACCELERATION	2001	TEST COND. E Y1 ORIENTATION ONLY	TEST COND. E Y1 ORIENTATION ONLY
D) SEAL	1014		
FINE LEAK		TEST COND. B	TEST COND. B
GROSS LEAK		TEST COND. C	TEST COND. C
E) VISUAL EXAMINATION	1010 & 1011		
F) END POINT ELECTRICAL.			
Sub 5 A) SALT ATMOSPHERE	1009	LTPD 15% S/S= 15 COND A C = 0	NOT BEING
B) VISUAL EXAMINATION	1009		
C) END POINT ELECTRICAL.			
Sub 6 INTERNAL WATER VAPOR CONTENT (5000 PPM)	1018	n = 3 : c = 0 or n = 5 : c = 1	NOT BEING
Sub 7 ADHESION OF LEAD FINISH	2025	LTPD 15% S/S = 15 C = 0	LTPD 15% S/S = 15 C = 0
Sub 8 LID TORQUE	2024	n = 5 : c = 0	n = 5 : c = 0

V. Group E : RADIATION HARDNESS ASSURANCE TESTS

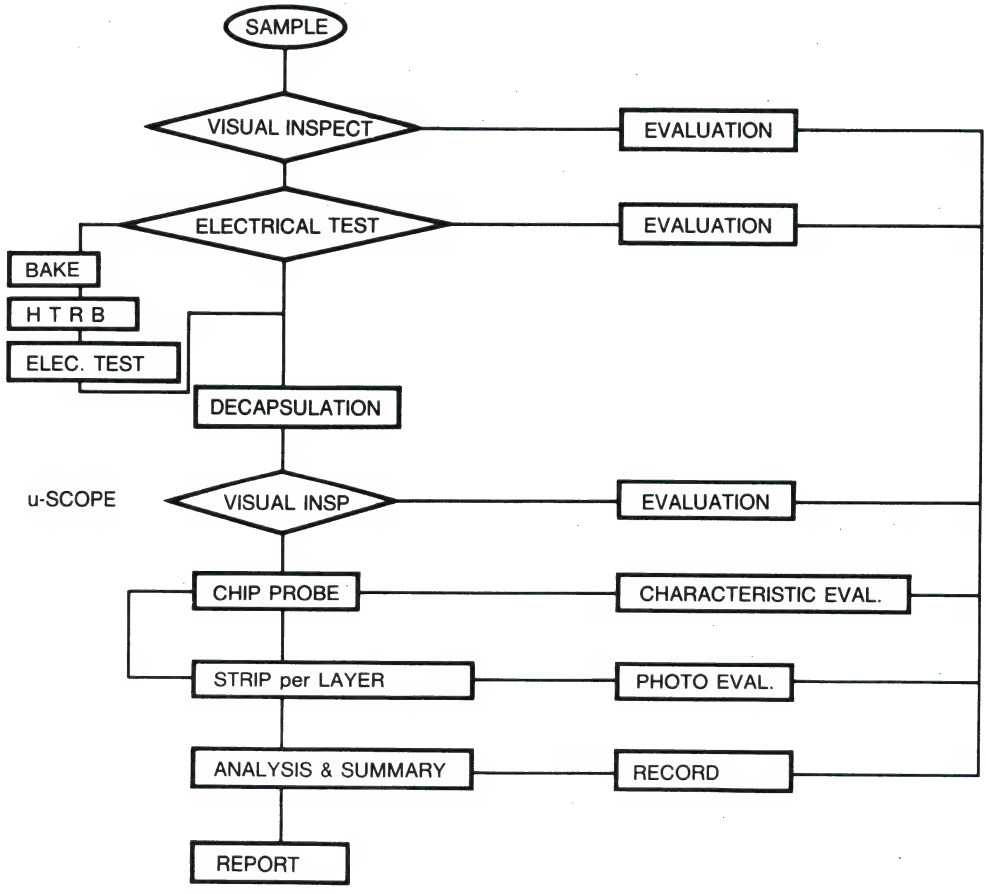
TEST ITEMS.	METHOD.	MIL-STD-883C	GOLDSTAR SEMI.
Sub 1			
NEUTRON IRRADIATION	1017	at 25°C	
A) QUALIFICATION		n = 15 : c = 0	NOT BEING
B) QCI		n = 11 : c = 0	
Sub 2			
STEADY-STATE TOTAL	1019	at 25°C	NOT BEING
DOSE IRRADIATION		n = 15 : c = 0	
A) QUALIFICATION		n = 11 : c = 0	
B) QCI			

FMA FLOW CHART

PROCEDURE OF FAILURE ANALYSIS



* FAILURE ANALYSIS



RELIABILITY TEST ITEMS of GOLDSTAR SEMICONDUCTOR

PLASTIC-DIP ONLY

ITEM	TEST ITEM	TEST CONDITION	QUALITY APPROVAL				QUALITY CONFORMANCE			
			TEST FREQ	S/S	LTPD	# of ACC.	TEST FREQ	S/S	LTPD	# of ACC.
1	Visual Inspection	Outgoing Visual Specification		—	—	—	Every Lot		AQL 0.065%	0
2	Electrical Test (DC/AC)	Outgoing Test Specification		—	—	—	Every Lot		AQL 0.04%	0
3	Dimension	Lead Thickness	Every Lot	5	—	0	Every Lot	1	—	0
4	Dimension	All Dimension	Every Week	5	—	0	Every Week	1	—	0
5	Packaging Inspection	Outging Packaging Specification		—	—	—	Every Lot	All	—	0
6	High Temperature Operating Life Test	Ta=125 C, t=1000 HRS Vcc=5V	Every 3 Month	77	5	1	Every Week	38	10	1
7	High Temperature Storage Test	Ta=150 C, t=1000 HRS	Every 3 Month	38	10	1		—	—	—
8	Biased Humidity Test	Ta=85 C 35% RH Vcc=5V, t=1000	Every 3 Month	38	10	1	Every Week	38	10	1
9	Pressure Pot	Ta=121 C, 30 PSIG 100% RH, 100 HRS	Every 3 Month	38	10	1	Every Week	25	15	0
10	Temperature Cycle Test	−65 C 25 C 150 C 10 Min, 5 Min, 10 Min 200 Cycle	Every 3 Month	38	10	1	Every Week	22	10	0
11	Lead Integrity	3 X, 90 Arcs 5 Units	Every 3 Month	15	15	0		—	—	—
12	Solderability	Solder Temp 240 5°C, Steam Aging 1 HRS Flux 6Sec, Solder 5Sec	2 Times / Weeks	22	10	0	2 Times / Weeks	22	10	0
13	Resistance to Solvents		Every Lot	15	15	0	Every Lot	15	15	0
14	Electro Static Discharge	MIC-STD-883C METHOD 3015	Every Lot	22	10	0	Every Lot	15	15	0

4. SUMMARY

This report has presented quality assurance system and reliability test on GoldStar Semiconductor devices. According to the reliability test results and actual experimental data of operating life test, it is concluded that GoldStar devices are high quality devices and the incoming failure rate is expected to be less than 0.04%.

5. HANDLING AND STORAGE INSTRUCTION

5.1 HANDLING PRECAUTIONS

For all devices, the following practices should be observed for protection against high electrical static discharges.

5.1.1 Device leads should be in contact with a conductive material except when being tested or in actual operation.

5.1.2 Conductive parts tools, fixtures, soldering irons and handling equipment should be grounded to handle the devices.

5.1.3 Devices should not be inserted into or removed from test stations unless the power is off.

5.1.4 Neither should signals be applied to the input while the device power supply is in an off condition.

5.1.5 Operators should use grounded wrist straps and work conductive surfaces should be also grounded.

5.2 STORAGING PRECAUTIONS.

There are several basic requirements in case of long term storage for semiconductor devices.

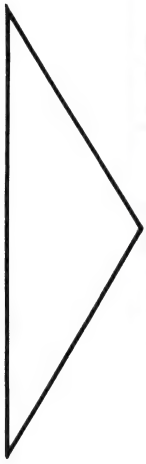
5.2.1 Store the devices in a covered or sealed antistatic container.

5.2.2 Store the devices in an enviroment of no more than 60% relative humidity.

5.2.3 Store the devices in a inert atmosphere not exceeding +125°C or no more than −55°C.

5.2.4 Physical force is not permitted on any leads or plastic body when the devices are stored for prevention damage of device.

NUMERICAL/FUNCTIONAL INDEX 1
FUNCTIONAL INDEX/SELECTION GUIDE 2
TTL CHARACTERISTICS 3
GD74LS FAMILY CIRCUITS 4
GD74S FAMILY CIRCUITS 5
QUALITY ASSURANCE MANUAL 6
ORDERING INFORMATION & PACKAGE DIMENSION 7
GOLDSTAR SEMICONDUCTOR SALES NETWORK 8



Ordering Information

Marking Code Formats of GS Biplar TTL are Shown as Following Example:

Ex:	GD	74	LS	373	A	P
	(1)	(2)	(3)	(4)	(5)	(6)

(1) GD: Prefix of GS Digital IC

(2) Operating Teperature Range
74; 0°C to + 70°C
54;−55°C to +125°C

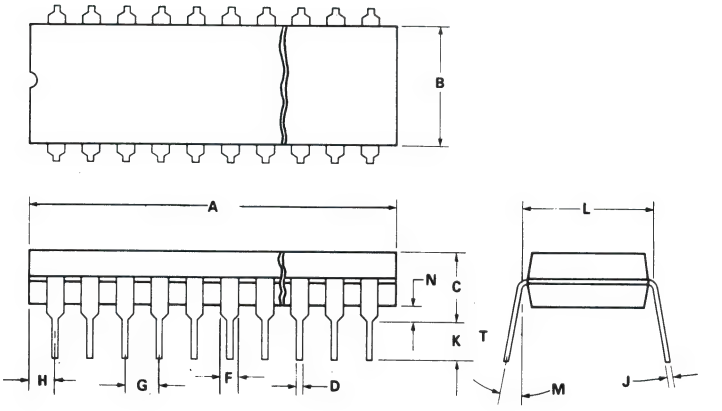
(3) Classification of TTL
LS: Low Power Schottky TTL
S: Schottky TTL

(4) Consecutive Number to Indicate the Each Type

(5) Alphabet: Series Impoved.

(6) Package Type
Blank : Plastic Dual In Line Package
J : Cermic Dual In Line Package
D : Small Outline Package

PLASTIC DIP



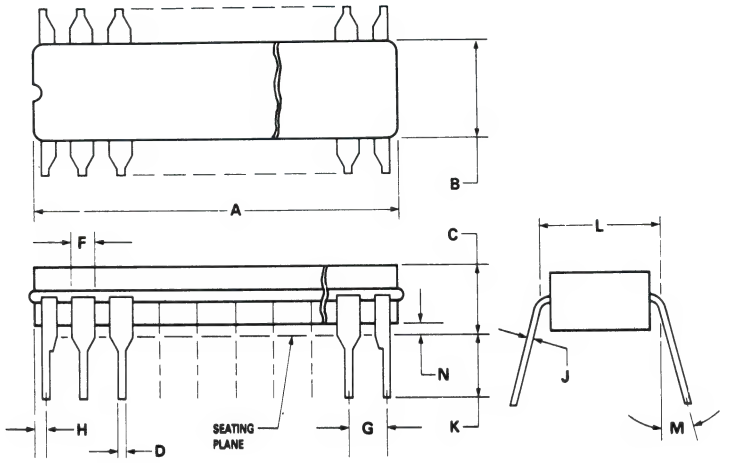
(INCHES)

SYMBOL	14 PIN		16 PIN		20 PIN		24 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.743	0.778	0.743	0.780	1.013	1.040	1.243	1.270
B	0.245	0.255	0.245	0.255	0.263	0.273	0.535	0.545
C	0.145	0.200	0.145	0.200	0.145	0.200	0.170	0.210
D	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
F	TYP 0.065		TYP 0.065		TYP 0.065		TYP 0.065	
G	0.09	0.11	0.09	0.11	0.09	0.11	0.09	0.11
H	—	0.075	0.015	0.045	0.055	0.065	0.06	0.09
J	0.009	0.015	0.009	0.015	0.009	0.015	0.009	0.015
K	0.125	0.140	0.125	0.140	0.125	0.140	0.125	0.140
L	0.300	0.320	0.300	0.320	0.300	0.320	0.6	0.62
M	0°	10°	0°	10°	0°	10°	0°	10°
N	0.02	—	0.02	—	0.02	—	0.015	—

(MILLIMETERS)

SYMBOL	14 PIN		16 PIN		20 PIN		24 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	18.87	19.56	18.87	19.81	25.73	26.42	31.57	32.26
B	6.223	6.477	6.223	6.477	6.477	6.731	13.589	13.843
C	3.683	5.080	3.683	5.080	3.683	5.080	4.318	5.234
D	0.387	0.527	0.387	0.527	0.387	0.527	0.387	0.527
F	TYP 1.524		TYP 1.524		TYP 1.524		TYP 1.524	
G	2.286	2.794	2.286	2.794	2.286	2.794	2.286	2.794
H	—	1.905	0.381	1.143	1.397	1.651	1.524	2.286
J	0.229	0.381	0.229	0.381	0.229	0.381	0.229	0.381
K	3.175	3.554	3.175	3.554	3.175	3.554	3.175	3.554
L	7.620	8.128	7.620	8.128	7.620	8.128	15.24	15.75
M	0°	10°	0°	10°	0°	10°	0°	10°
N	5.08	—	5.08	—	5.08	—	3.81	—

CERAMIC DIP



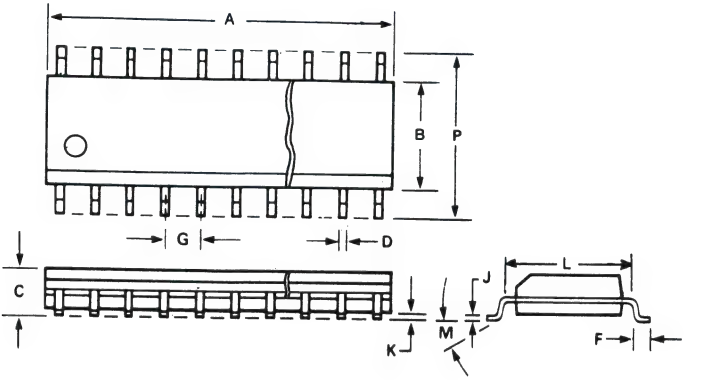
(INCHES)

SYMBOL	14 PIN		16 PIN		20 PIN		24 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	—	0.785	—	0.785	—	0.985	—	1.290
B	0.22	0.31	0.22	0.31	0.22	0.31	0.514	0.526
C	—	0.18	—	0.18	—	0.18	—	0.18
D	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
F	0.055	0.065	0.055	0.065	0.050	0.060	0.055	0.065
G	0.09	0.11	0.09	0.11	0.09	0.11	0.09	0.11
H	—	0.098	—	0.08	—	0.08	—	0.098
J	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
K	0.125	0.20	0.125	0.20	0.125	0.20	0.125	0.20
L	0.29	0.32	0.29	0.32	0.29	0.32	0.59	0.62
M	0°	10°	0°	10°	0°	10°	0°	10°
N	0.02	0.06	0.02	0.06	0.02	0.07	0.02	0.06

(MILLIMETERS)

SYMBOL	14 PIN		16 PIN		20 PIN		24 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	—	19.939	—	19.939	—	25.019	—	32.766
B	5.588	7.784	5.588	7.784	5.588	7.784	13.06	13.36
C	—	4.572	—	4.572	—	4.572	—	4.572
D	0.387	0.527	0.387	0.527	0.387	0.527	0.387	0.527
F	1.397	1.651	1.397	1.651	1.27	1.524	1.397	1.651
G	2.286	2.794	2.286	2.794	2.286	2.794	2.286	2.794
H	—	2.489	—	2.032	—	2.489	—	2.489
J	0.203	0.305	0.203	0.305	0.203	0.305	0.203	0.305
K	3.175	5.080	3.175	5.080	3.175	5.080	3.175	5.080
L	7.366	8.128	7.366	8.128	7.366	8.128	14.986	15.748
M	0°	10°	0°	10°	0°	10°	0°	10°
N	0.051	0.152	0.051	0.152	0.051	0.178	0.051	0.152

SOIC



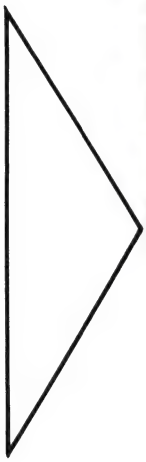
(INCHES)

SYMBOL	14 PIN		16 PIN		20 PIN		24 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.337	0.344	0.386	0.394	0.496	0.510	0.598	0.614
B	0.15	0.157	0.15	0.157	0.291	0.299	0.291	0.299
C	0.053	0.069	0.053	0.069	0.093	0.104	0.093	0.104
D	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
F	0.027	0.035	0.027	0.035	0.027	0.035	0.034	0.042
G	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC	
J	0.007	0.010	0.007	0.010	0.009	0.013	0.009	0.013
K	0.004	0.008	0.004	0.008	0.004	0.008	0.004	0.008
L	0.189	0.205	0.189	0.205	0.368	0.375	0.368	0.375
P	0.228	0.244	0.228	0.244	0.404	0.419	0.404	0.419
M	0°	8°	0°	8°	0°	8°	0°	8°

(MILLIMETERS)

SYMBOL	14 PIN		16 PIN		20 PIN		24 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	8.55	8.75	9.80	10.10	12.60	13.00	15.20	15.60
B	3.80	4.00	3.80	4.00	7.40	7.60	7.40	7.60
C	1.35	1.75	1.35	1.75	2.35	2.65	2.35	2.65
D	0.35	0.49	0.35	0.49	0.35	0.49	0.35	0.49
F	0.69	0.89	0.69	0.89	0.86	1.07	0.86	1.09
G	1.27 BSC		1.27 BSC		1.27 BSC		1.27 BSC	
J	0.19	0.25	0.19	0.25	0.23	0.32	0.23	0.32
K	0.10	0.20	0.10	0.20	0.10	0.20	0.10	0.20
L	4.82	5.21	4.82	5.21	9.34	9.53	9.34	9.53
P	5.80	6.20	5.80	6.20	10.26	10.65	10.26	10.65
M	0°	8°	0°	8°	0°	8°	0°	8°

NUMERICAL/FUNCTIONAL INDEX 1
FUNCTIONAL INDEX/SELECTION GUIDE 2
TTL CHARACTERISTICS 3
GD74LS FAMILY CIRCUITS 4
GD74S FAMILY CIRCUITS 5
QUALITY ASSURANCE MANUAL 6
ORDERING INFORMATION & PACKAGE DIMENSION 7
GOLDSTAR SEMICONDUCTOR SALES NETWORK 8



GOLDSTAR SEMICONDUCTOR SALES NETWORK

ASIA

KOREA

° KUM SUNG JUN SIN ELECTRONICS CO,. LTD.
182-13, Jangsa-Dong, Chongro-Gu
Seoul, Korea
Tel:02-273-6811-3/274-1911-2
Fax:02-272-4367

° NAM SUNG ELECTRONICS
70-12 Goe-Dong Choong-Gu
Daegu, Korea
Tel:053-423-0654
Fax:053-423-6689

° SAM JIN ELECTRONICS
671-1, Junpo 1 Dong Busanjingu
Busan, Korea
Tel:051-807-1717 / 1747
Fax:051-807-6657

° SEOG YUNG ELECTRONICS
182-2, Jangsa-Dong, Chongro-Gu
Seoul, Korea
Tel:02-273-6781
Fax:02-273-6597

° SOKCHUN TRADING CO.,LTD.
3112 Sun-In B/D Young San
K.P.O.Box 1148, Seoul, Korea
Tel:02-273-7877,266-1940
701-7811/7814
Fax:02-274-3291

° WOO SUNG SEMICONDUCTOR
5005Ho 22Dong Seonin Sangga
16-1, Hangangro-2Ga, YongSan-Gu
Seoul, Korea
Tel:02-273-4730, 272-3874
701-0291-4
Tlx:WOOSEM K28711
Fax:02-701-0295

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* GOLDSTAR (H.K.) LTD.
Rm. 1501B, World Wide House,
19, Des Voeux Road, Central,
Hong Kong.
Tel:5-8456787
Tlx:89860 GSH HX
Fax:5-8459416

* LUCKY-GOLDSTAR INT'L LTD.
Rm. 3001, Gloucester Tower
30th Fl. The Landmark
Central, Hong Kong
Tel:5-266402/7
Tlx:62711 LGI HX
Fax:5-8681460

• FUTURISTIC ELECTRONICS CO., LTD.
Flat.A-11,7/F Tonic Industrial Center
No.26, Kai Cheung Rd. Kowloon Bay
Kowloon,H.K.
Tel:3-796-7968
Tlx:52882 FETSC HX
Fax:3-796-7420

• SUN COMPONENTS LTD.
1/F Hang Lung Bank Bldg.
46-48 Granville Road
Tsim Sha Tsui, Kowloon, H.K.
Tel:852-3-3118321
Tlx:55858 ONFLO HX
Fax:852-3-311-6715

• TECHGROW LTD.
4B Cheerful Comm. Bldg.
116-118, Ma Tau Wai Rd. Hunghom,
Kowloon
Hong Kong
Tel:3-764-3618
Tlx:32465 TGL HX
Fax:3-764-1781

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* GOLDSTAR CO., LTD.
Room 306-309 Parkash Deep Bldg.
7, Tolstoy Marg.
New Delhi 110 001, India
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Tlx:3161599 LGND IN
Fax:91-11-3323754

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Tlx:3161599 LGND IN
Fax:91-11-3323754

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15, Amrut Hansoti Rd.
Cama lane, Ghatkopar (W)
Bombay 400 086, India
Tel:91-22-5114789
Tlx:1172313 SMC IN
Fax:91-22-5136940

• SPARTEX SYSTEMS & SERVICES PVT. LTD.
No. 68, Michael Palyam,
Near Deccan Studio, C.V. Raman Nagar
Post
Bangalore 560 093, India
Tel:91-812-564211
Tlx:8452190 MLHR IN

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* GOLDSTAR JAPAN CO., LTD.
Hon-Kan 9F. Akasaka Twin Tower
17-22, 2-Chome, Akasaka, Minato-ku
Tokyo, Japan
Tel:03-224-0123
Tlx:J22873 GSTOKYO
Fax:03-582-7948

• JAPAN MACNICS CORP.
516, Imaiminami-Cho, Nakahara-Ku
Kawasaki-City, Kanagawa-Ken, 211
Japan
Tel:044-711-0022
Tlx:28988 JAPMAC J
Fax:044-711-2214

• OHTORI CORP.
9-8, 5 Chome,
Nipponbashi, Naniwa-Ku,
Osaka Japan
Tel:06-643-1655
Tlx:526-7218
Fax:06-633-5212

• OKAMOTO MUSEN CO., LTD. TOKYO BRANCH
3-2-17 Nozawa, Setagay-Ku
Tokyo 154, Japan
Tel:03-412-8211
Fax:03-418-2555

SINGAPORE

* GOLDSTAR CO., LTD.
8 Shenton Way
#30-04 Treasury Bldg.
S'pore 0106
Tel:65-2243166
Tlx:RS 29118 GSSPO
Fax:65-2240721

* LUCKY-GOLDSTAR INT'L CORP.
8 Shenton Way
#39-03 Treasury Bldg.
S'pore 0106
Tel:65-2204566
Tlx:RS 33922 LGTSPO
Fax:65-2249049

• DYNAMAR HOLDINGS PTE LTD.
109 Defu Lane 10
Singapore 1953
S'pore 1334
Tel:281-3388
Tlx:RS 26283 DYNAMA
Fax:281-3308

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° : Sales Distributors
¤ : Sales Representatives
• : Sales Representatives/Distributors

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•DYNAMAR COMPUTER PRODUCTS CO., LTD.
444 Ratchadapisek Road Samsennok
Hauy Kwang Bangkok 10310
Thailand
Tel:662-511-5104, 511-4809, 511-4331
Fax:662-512-1067

TAIWAN

* GOLDSTAR CO., LTD. TAIPEI OFFICE
3F-4, No. 695, Tun Hwa South Road, Taipei
Taiwan, R.O.C.
Tel:02-755-6658
Fax:02-702-0687

* LUCKY-GOLDSTAR INT'L CORP.
3F-4, NO. 695
Tun Hwa South Road, Taipei,
Taiwan, R.O.C.
Tel:02-755-6648/6650
Fax:02-702-0687

•BRIGHT UP INDUSTRIES CO., LTD.
12F, N0. 142, Chung-Hsiao
E. Rd. SEC. 4 Taipei, Taiwan, R.O.C.
Tel:02-773-2194/8, 776-5455/9
Fax:02-751-9545

•GOLDEN SEVEN ENTERPRISE CO., LTD.
10th Fl. #95-1 Sung Chiang Rd. Taipei,
Taiwan, R.O.C.
Tel:02-507-1186
Tlx:26140 GOSEVEN
Fax:02-508-2250

•LUMAX INT'L CORP., LTD.
14th Fl., 687 Ming Sheng East Rd.
Taipei, Taiwan, R.O.C.
Tel:02-715-5976
Fax:02-716-4649
Tlx:22607 LUMAX

•UNITECH DEVICE CORP.
6F-2,No.142,Chung-Hsiao
E. Rd. SEC. 4 Taipei, Taiwan, R.O.C.
Tel:02-7760560/5
Fax:02-7313100

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* LUCKY-GOLDSTAR INT'L CORP.
Mariahilfer Strasses 77-79,
1060, Wien, Austria
Tel:222-933747
Tlx:134419 LG INTA
Fax:222-933739

° E.S.L. HANDELSGES M.B.H.
Wasagasse 26/3B
A-1090,Wien, Austria
Tel:222-310-1025
Tlx:135548 ESL A
Fax:222-310-1027

BELGIUM

° MALCHUS ELECTRONICS
Plantin-moretusiei 172
B-2018 Antwerpen, Belgium
Tel:3-2353272
Tlx:33637 MALCH B
Fax:3-2711049

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° OLE WOLFF ELEKTRONIK APS.
Rodengvej 25, Dk 4180 Soro.
Denmark
Tel:3-633830
Tlx:40294 WOLFF DK
Fax:3-630183

FINLAND

° ELDIS OY
Niittyrinne 6, 02270, Espoo, Finland
Tel:0-8039044
Tlx:121278 ELDIS SF
Fax:0-8039089

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* LUCKY-GOLDSTAR INT'L CORP.
PARIS OFFICE
24, Avenue De La Grande-Armee
75017 Paris, France
Tel:1-4766-8888
Tlx:640221F LGIPAR
Fax:1-4766-1380

¤ AGEREP
7, rue Marcelin Berthelot
92160 ANTONY, France
Tel:1-4666-8033
Tlx:204871 GEPSI
Fax:1-4096-9226

° COMPTOIR COMMERCIAL D'IMPORTATION
5, rue Marcelin Berthelot
92160 Antony, France
Tel:1-4666-2182
Tlx:LORESOL 203881
Fax:1-4096-9226

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° DAEWON EUROPA S.R.L.
Via lenardo da vinci, 43
20090 Trezzano Sul Naviglio
(Milano), Italy
Tel:2-4450042
Tlx:323261 DWESKP
Fax:2-4450184

° MELCHIONI S.P.A.
Via P. Colletta,37
20135 Milano, Italy
Tel:2-57941
Tlx:320321 MELKIO I
Fax:2-5461081

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° MALCHUS B.V.
P.O. Box 4S
3100AA Schiedem, Netherlands
Tel:10-4277777
Tlx:21598 MALCH NL
Fax:10-4154867

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° FEIRING ELEKTRONIKK A/S
P.O. Box 101, Bryn,
0611 Oslo 6, Norway
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Tlx:74592 FEIIK N
Fax:2-644051

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° INDUTRONIK,S.A.
Angelita Cavero,9
28027 Madrid, Spain
Tel:1-741-8011
Tlx:47821 INTK E
Fax:1-742-6831

° LOBER, S,A.
Monte Esquinza, 28
E-28010 Madrid, Spain
Tel:1-410-6821
Tlx:49533 TLOB E
Fax:1-410-6968

* : Sales Offices
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¤ : Sales Representatives
● : Sales Representatives/Distributors

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° MIKO KOMPONENT AB
Seger Sbyvagen 3
S-14502 Norsborg, Sweden
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Tlx:15023 MIKO S
Fax:753-75340

SWITZERLAND

° ETRONICS AG
Sonnenberg, P.O.B.23
8103 Unterengstringen, Switzerland
Tel:1-750-3511
Tlx:829055 AETR CH
Fax:1-750-3567

TURKEY

° COMTEC San. ve Tic. Koll. Sti.
Hasanpasa, Ahmet Rasim Sok,
No. 16 Kadikoy Istanbul, Turkey
Tel:1-337-2245
Tlx:29569 ELTS TR
Fax:1-336-8814

U.K.

* GOLDSTAR CO., LTD.
Goldstar House 264 Bath
Road Slough Berkshire Sli 4EW
Tel:44-753-691888
Tlx:846284 GSUK G
Fax:44-753-693061

* LUCKY-GOLDSTAR INT'L (U.K.)LTD.
1-Fl, Califton House 83-89
Uxbridge Rd. Ealing
London W5 5TA, U.K.
Tel:840-7111
Tlx:21765 LGIUK G
Fax:840-1658

° KORD DISTRIBUTION LTD.
Watchmoor Road Camberley
Surrey GU15 3AQ., U.K.
Tel:276-685741
Tlx:859919 KORDIS G
Fax:276-691334

W. GERMANY

* GOLDSTAR Deutschland GmbH
Zentrale Ratingen
HarkortstraBe 41
D-4030 Ratingen
Tel:02102-4987-0
Tlx:8585262 GSDG D
Fax:02102-49-9662

* LUCKY-GOLDSTAR INT'L (Deutschland) GmbH
Lyoner Stern Bldg.
Hahnstrasse 70
D-6000 Frankfurt Am Main 71
W.Germany
Tel:69-663-0070
Tlx:4185337 LGIF D
Fax:69-666-6865

° BECK GmbH & CO. ELEKTRONIK
Bnauelemente KG. Postfach
91,02 80 8500 Nuernberg 91, W.Germany
Tel:0911-34050
Tlx:622334 BECK D
Fax:0911-340528

OCEANIA

AUSTRALIA

° NOVOCASTRIAN ELECTRONIC SUPPLIES PTY LTD.
24 Broadmeadow Rd. Broadmeadow
NSW, 2292, Australia
Tel:49-62-1358
Fax:49-62-2005

AFRICA

EGYPT

° HELIOPOLIS EST FOR IMPORT AND ELECTRICAL CONTRACTS
13 El Somal St. El Korpa, Heliopolis
P.O. Box 610 H.W.
Tel:660793/674986
Tlx:20348 MOMA

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U.S.A.

* GOLDSTAR TECHNOLOGY, INC.
1130 East Arques Avenue,
Sunnyvale CA 94086
Tel:408-737-8575
Fax:408-737-0186

* GOLDSTAR TECHNOLOGY, INC. EASTERN AREA OFFICE
1821 Walden Office Square, Suite 426
Schaumberg, IL 60173
Tel:312-397-0004
Fax:312-303-1121

* GOLDSTAR TECHNOLOGY, INC. WESTERN AREA OFFICE
6576 Corte Cisco
Carisbad. CA 92008
Tel:619-931-7641
Fax:619-931-9628

ALABAMA

¤ EMA WESTERN REGIONAL OFFICE
309 Jordan Lane N.W.
Huntsville, AL 35805
Tel:205-830-4030
Fax:205-830-1947

° RESISTACAP, INC.
P.O. Box 14069
11547 S.Memorial Parkway
Huntsville, AL 35815
Tel:205-883-4270
Fax:205-881-7624

ARIZONA

° ADDED VALUE ELECTRONIC DISTRIBUTION, INC.
7741 East Gray Road. Suite #9
Scottsdale. AZ 85260
Tel:602-951-9788
Fax:602-951-4182

CALIFORNIA

¤ HADDEN ASSOCIATES, INC.
4710 Rusner St. Suite H
San Diego, CA 90111
Tel:619-565-1944
Fax:619-565-1802

¤ MAGNA SALES
3333 Bowers. Suite 251
Santa Clara, CA 95054
Tel:408-727-8753
Fax:408-727-8573

° ADDED VALUE ELECTRONIC DISTRBUIION, INC.
6397 Nancy Ridge Road
San Diego, CA 92121
Tel:619-558-8890
Fax:619-558-3018

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● : Sales Representatives/Distributors

GOLDSTAR SEMICONDUCTOR SALES NETWORK

° ALL AMERICAN SEMICONDUCTOR, INC.
2360 Qume Drive, Suite B
San Jose, CA 95131
Tel:408-943-1200
800-222-6001
Fax:408-943-1393

° JACO ELECTRONICS, INC.
2880 Zanker, Suite 202
San Jose, CA 95134
Tel:408-432-9290
Fax:408-432-9298

° CYPRESS ELECTRONICS
2175 Martin Ave.
Santa Clara, CA 95050
Tel:408-980-2500
Fax:408-986-9584

° ALL AMERICAN SEMICONDUCTOR, INC.
369 Van Ness Way, #701
Torrance, CA 90501
Tel:213-320-0240
800-669-8300
Fax:213-320-7207

° ADDED VALUE ELECTRONIC DISTRIBUTION, INC.
1582 Parkway Loop, Unit G
Tustin. CA 92680
Tel:714-259-8258
Fax:714-259-0828

° ADDED VALUE ELECTRONIC DISTRIBUTION, INC.
3320 East Mineral King, Unit D
Visalia, CA 93291
Tel:209-734-8861
Fax:209-734-8865

° ADDED VALUE ELECTRONIC DISTRIBUTION, INC.
31194 LaBaya #100
Westlake Village. CA 91362
Tel:818-889-2861
Fax:818-889-2472

COLORADO

° A.V.E.D.-ROCKY MOUNTAIN, INC.
4090 Youngfield Street
Wheat Ridge, CO 80033
Tel:303-422-1701
Fax:303-422-2529

CONNECTICUT

° PARK DISTRIBUTORS
347 Railroad Avenue
Bridgeport, CT 06604
Tel:203-366-7200
Fax:205-881-7624

FLORIDA

¤ LAWRENCE ASSOCIATES, INC.
711 Turnbull Avenue
Altamonte Springs, FL 32701
Tel:407-339-3855
Fax:407-767-0973

¤ LAWRENCE ASSOCIATES, INC.
5021 N.Dixie Hwy.
Boca Raton, FL 33431
Tel:407-368-7373
Fax:407-394-5441

¤ LAWRENCE ASSOCIATES, INC.
1417 Malabar Lakes Drive N.E.
Palm Bay, FL 32905
Tel:407-984-0669
Fax:407-951-0906

¤ LAWRENCE ASSOCIATES, INC.
1131 US 19 South
Palm Harbor, FL 34864
Tel:813-787-2773
Fax:813-787-2654

° ALL AMERICAN SEMICONDUCTOR, INC.
16251 N.W. 54th Avenue
Miami. FL 33014
Tel:305-621-8282
Fax:305-620-7831

° ALL AMERICAN SEMICONDUCTOR, INC.
5009 Hiatus Road
Sunrise, FL 33351
Tel:305-572-7999
Inside FL: 800-432-6838
Outside FL: 800-327-6237
Fax:305-749-9229

° JACO ELECTRONICS, INC.
1202 Tech. Blvd., Suite 201
Tampa. FL 33619
Tel:813-628-4665
Toll Free from N.FL & GA:800-265-JACO
Fax:813-626-8185

GEORGIA

¤ EMA
EASTERN REGIONAL OFFICE
620 Colonial Park Drive
Roswell, GA 30075
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Fax:404-993-3426

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¤ TRISTAR
930 Lee St.
Elk Grove Village, IL 60007
Tel:312-593-0200
Fax:312-364-6507

° ADVENT ELECTRONICS, INC.
7110-16N. Lyndon Street
Rosemont, IL 60018
Tel:312-298-4210
Fax:312-297-6650

° Q.P.S. ELECTRONICS, INC.
101 East Commerce Dr.
Schaumberg, IL 60173
Tel:312-884-6620

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